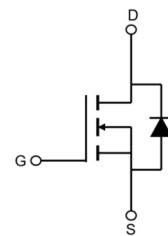


Feature

- 200V,5A
- $R_{DS(on)} < 500\text{m}\Omega @ V_{GS}=10\text{V}$ TYP:430 mΩ
- Advanced Trench Technology
- Lead free product is acquired
- Excellent $R_{DS(on)}$ and Low Gate Charge



Schematic Diagram



Marking and pin assignment

Application

- PWM applications
- Load Switch
- Power management

Package Marking and Ordering Information

Device Marking	Device	Device Package	Reel Size	Tape width	Quantity (PCS)
5N20K	AP5N20K	TO-252	13 inch	-	2500

ABSOLUTE MAXIMUM RATINGS ($T_a=25^\circ\text{C}$ unless otherwise noted)

Parameter	Symbol	Value	Unit
Drain-Source Voltage	V_{DS}	200	V
Gate-Source Voltage	V_{GS}	± 20	V
Continuous Drain Current ($T_a = 25^\circ\text{C}$)	I_D	5	A
Continuous Drain Current ($T_a = 100^\circ\text{C}$)	I_D	3.3	A
Pulsed Drain Current ⁽¹⁾	I_{DM}	20	A
Singel Pulsed Avalanche Energy ⁽²⁾	E_{AS}	125	mJ
Power Dissipation	P_D	78	W
Thermal Resistance from Junction to Case	R_{eJC}	1.6	°C/W
Junction Temperature	T_J	150	°C
Storage Temperature	T_{STG}	-55~+150	°C

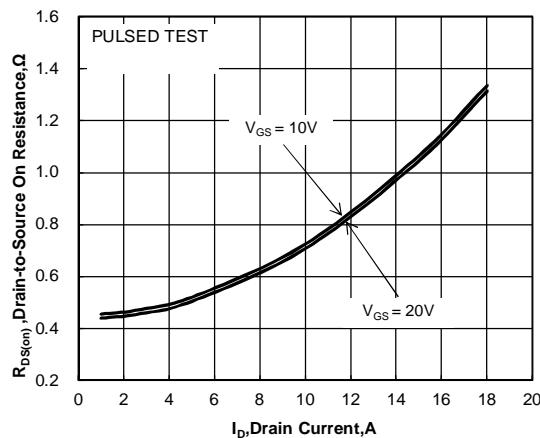
MOSFET ELECTRICAL CHARACTERISTICS($T_a=25^\circ\text{C}$ unless otherwise noted)

Parameter	Symbol	Test Condition	Min	Type	Max	Unit
Static Characteristics						
Drain-source breakdown voltage	$V_{(\text{BR})\text{DSS}}$	$V_{\text{GS}} = 0\text{V}, I_{\text{D}} = 250\mu\text{A}$	200	-	-	V
Zero gate voltage drain current	I_{DSS}	$V_{\text{DS}} = 200\text{V}, V_{\text{GS}} = 0\text{V}$	-	-	1	μA
Gate-body leakage current	I_{GSS}	$V_{\text{GS}} = \pm 20\text{V}, V_{\text{DS}} = 0\text{V}$	-	-	± 100	nA
Gate threshold voltage ⁽³⁾	$V_{\text{GS}(\text{th})}$	$V_{\text{DS}} = V_{\text{GS}}, I_{\text{D}} = 250\mu\text{A}$	1	1.6	2.5	V
Drain-source on-resistance ⁽³⁾	$R_{\text{DS}(\text{on})}$	$V_{\text{GS}} = 10\text{V}, I_{\text{D}} = 2.5\text{A}$	-	430	500	$\text{m}\Omega$
Forward transconductance ⁽³⁾	g_{FS}	$V_{\text{DS}} = 30\text{V}, I_{\text{D}} = 2.5\text{A}$	-	5.2	-	S
Dynamic characteristics						
Input Capacitance	C_{iss}	$V_{\text{DS}} = 25\text{V}, V_{\text{GS}} = 0\text{V}, f = 100\text{kHz}$	-	255	-	pF
Output Capacitance	C_{oss}		-	30.2	-	
Reverse Transfer Capacitance	C_{rss}		-	2.3	-	
Switching characteristics						
Turn-on delay time	$t_{\text{d}(\text{on})}$	$V_{\text{DD}} = 100\text{V}, I_{\text{D}} = 5\text{A}, V_{\text{GS}} = 10\text{V}, R_{\text{G}} = 2\Omega$	-	7.33	-	ns
Turn-on rise time	t_{r}		-	10.7	-	
Turn-off delay time	$t_{\text{d}(\text{off})}$		-	18.2	-	
Turn-off fall time	t_{f}		-	11.9	-	
Total Gate Charge	Q_{g}	$V_{\text{DS}} = 100\text{V}, I_{\text{D}} = 5\text{A}, V_{\text{GS}} = 10\text{V}$	-	10.8	-	nC
Gate-Source Charge	Q_{gs}		-	1.7	-	
Gate-Drain Charge	Q_{gd}		-	3.1	-	
Source-Drain Diode characteristics						
Diode Forward voltage ⁽³⁾	V_{DS}	$V_{\text{GS}} = 0\text{V}, I_{\text{s}} = 1\text{A}$	-	-	1.4	V
Diode Forward current ⁽⁴⁾	I_{s}		-	-	5	A

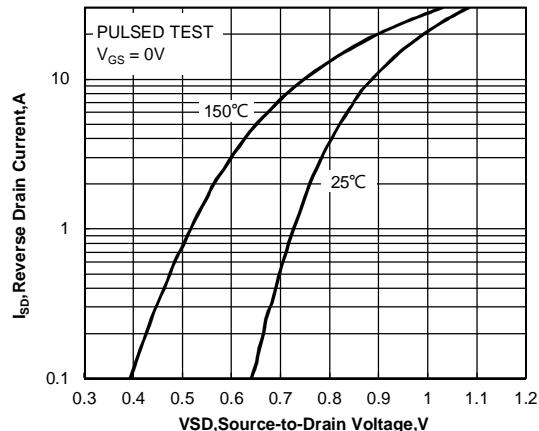
Notes:

1. Repetitive Rating: pulse width limited by maximum junction temperature
2. EAS Condition: $T_J=25^\circ\text{C}, V_{\text{DD}}=50\text{V}, R_{\text{G}}=50\Omega, L=0.5\text{mH}$
3. Pulse Test: pulse width $\leq 300\mu\text{s}$, duty cycle $\leq 2\%$
4. Surface Mounted on FR4 Board, $t \leq 10$ sec

Typical Performance Characteristics



**Figure 1. Drain-to-Source On Resistances.
Drain Current and Gate Voltage**



**Figure 2. Body Diode Forward Voltages.
Source Current and Temperature**

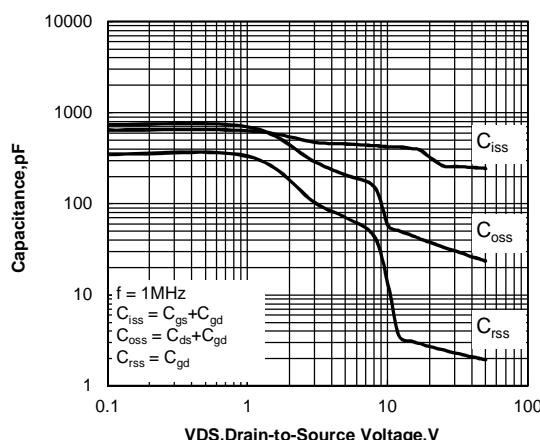


Figure 3. Capacitance Characteristics

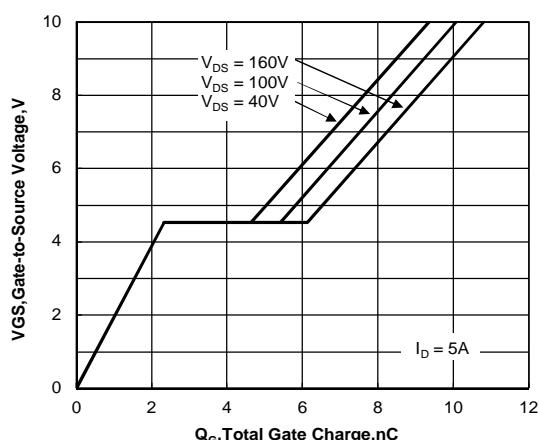


Figure4 . Gate Charge Characteristics

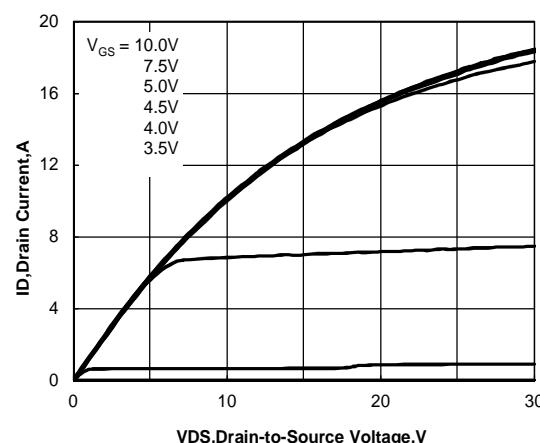
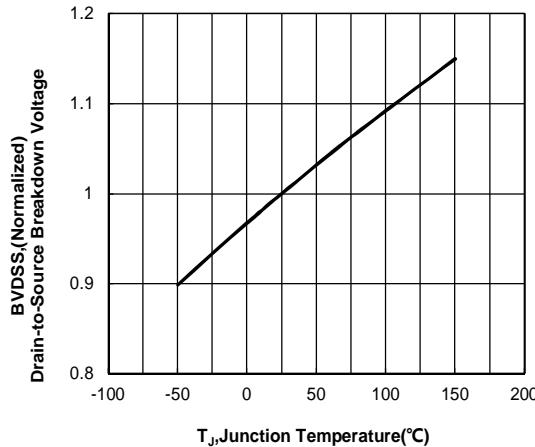
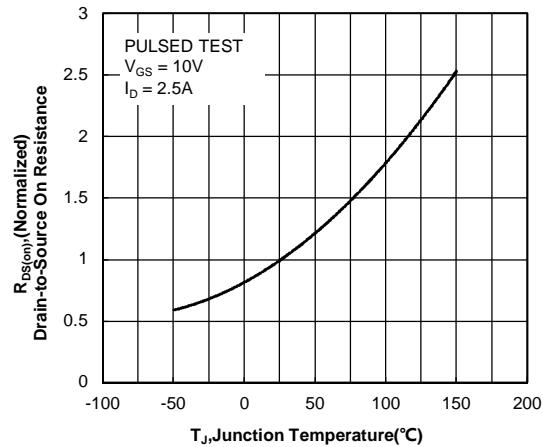


Figure 5. Output Characteristics



**Figure 6. Normalized Breakdown Voltage vs.
Junction Temperature**



**Figure 7. Normalized On Resistance vs.
Junction Temperature**

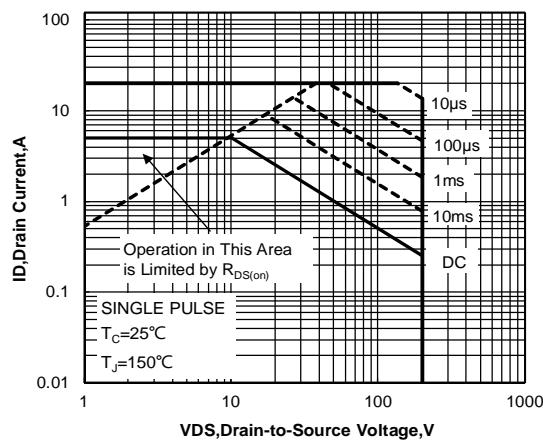
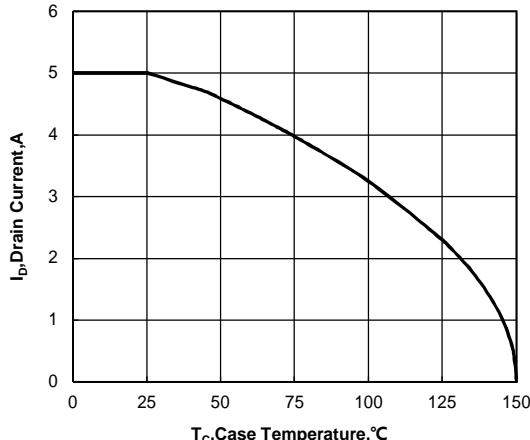


Figure 8. Maximum Safe Operating Area for AP5N20A



**Figure 9. Maximum Continuous Drain Current vs.
Case Temperature**

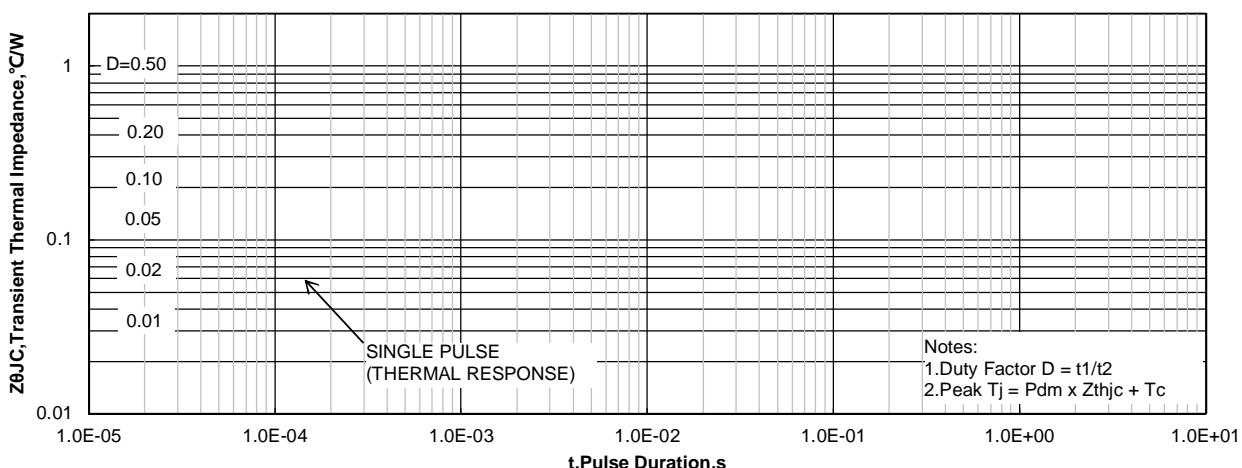


Figure 10. Maximum Effective Transient Thermal Impedance, Junction-to-Case for AP5N20A

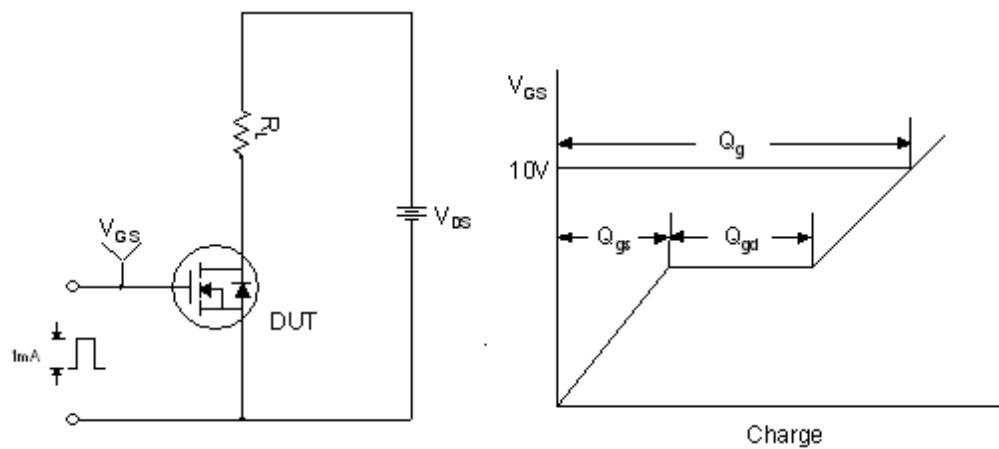


Figure 11. Gate Charge Test Circuit & Waveform

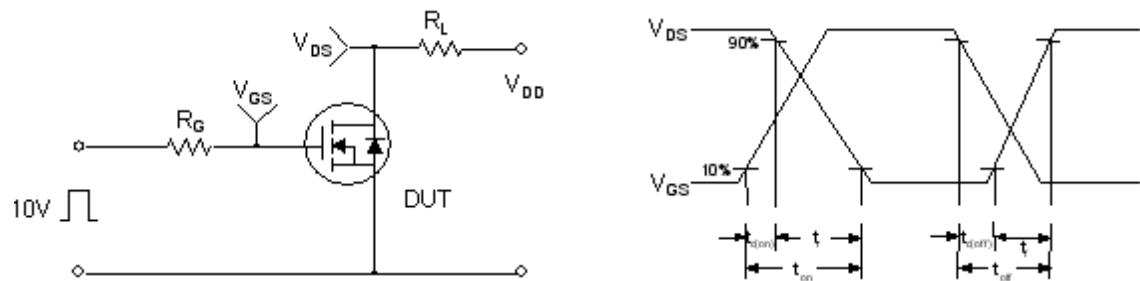


Figure 12. Resistive Switching Test Circuit & Waveforms

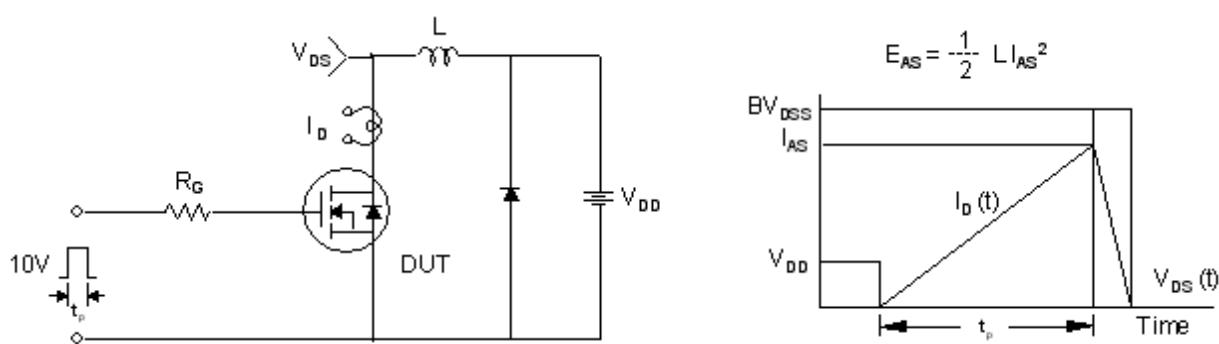


Figure 13. Unclamped Inductive Switching Test Circuit & Waveforms

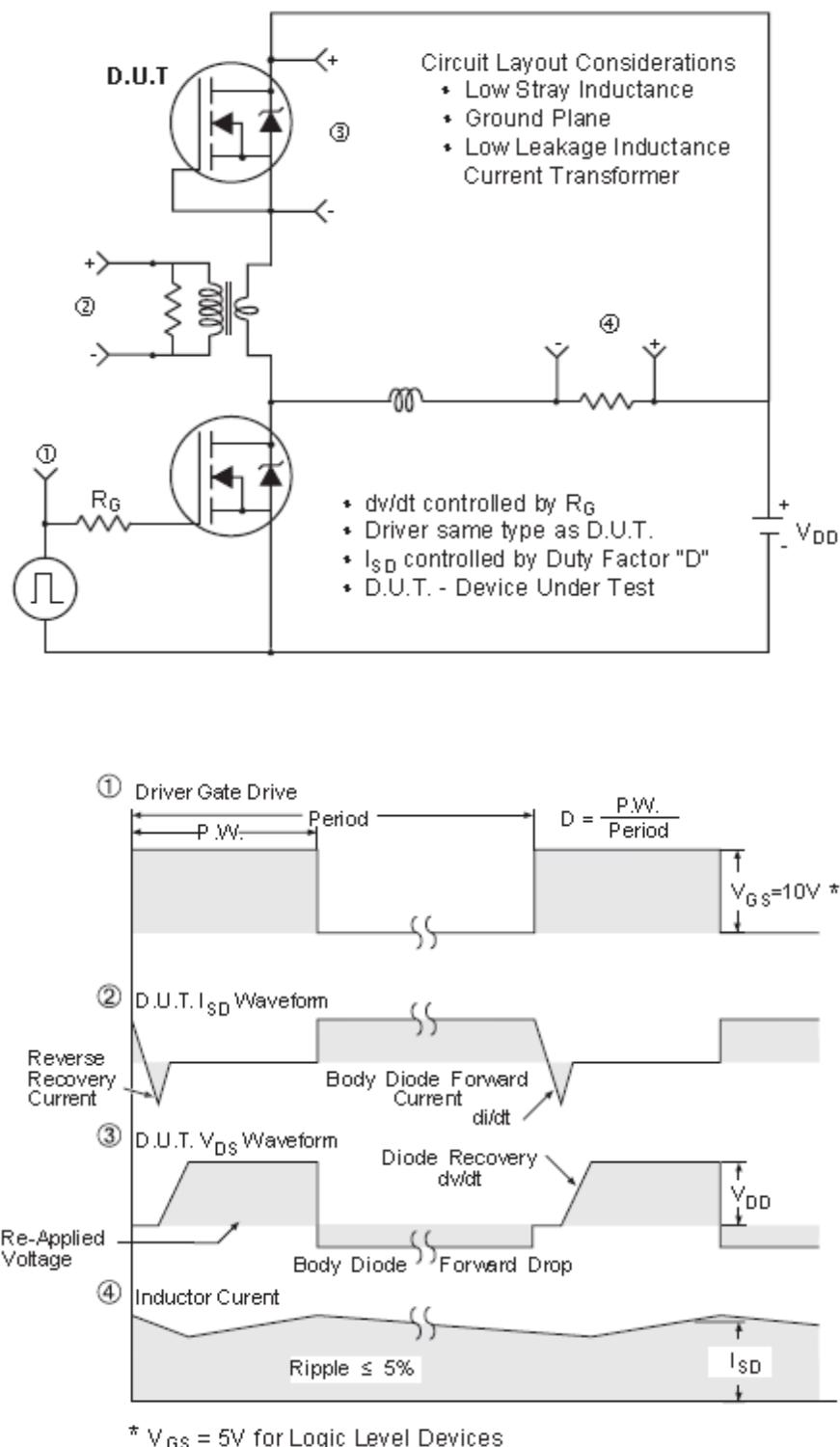
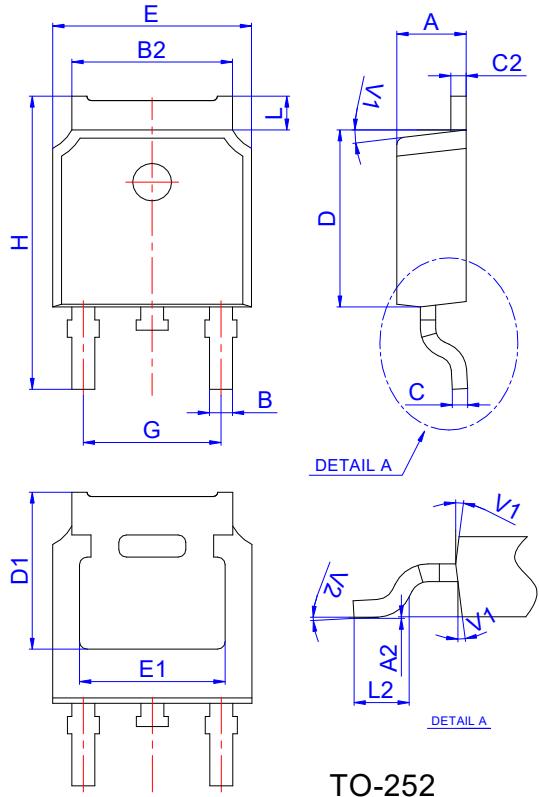


Figure 14. Peak Diode Recovery dv/dt Test Circuit & Waveforms (For N-channel)

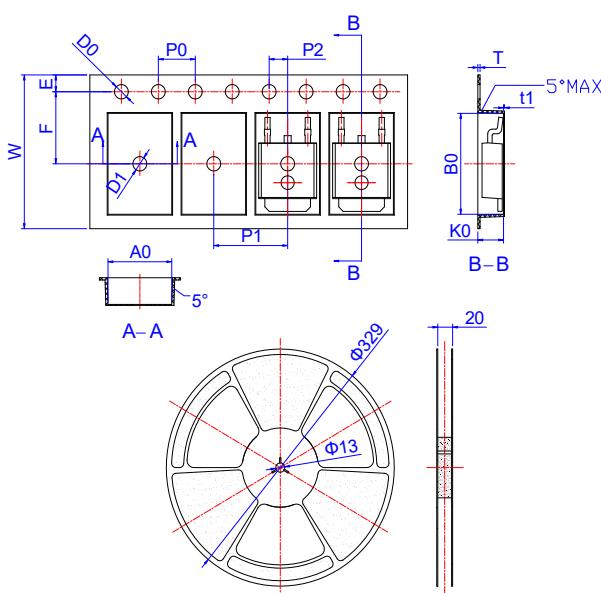
TO-252 Package Information



TO-252

Ref.	Dimensions					
	Millimeters			Inches		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A	2.10			2.50	0.083	
A2	0			0.10	0	0.004
B	0.66			0.86	0.026	0.034
B2	5.18			5.48	0.202	0.216
C	0.40			0.60	0.016	0.024
C2	0.44			0.58	0.017	0.023
D	5.90			6.30	0.232	0.248
D1	5.30REF			0.209REF		
E	6.40			6.80	0.252	
E1	4.63				0.182	
G	4.47			4.67	0.176	0.184
H	9.50			10.70	0.374	0.421
L	1.09			1.21	0.043	0.048
L2	1.35			1.65	0.053	0.065
V1		7°				7°
V2	0°			6°	0°	6°

Reel Specification-TO-252



Ref.	Dimensions					
	Millimeters			Inches		
	Min.	Typ.	Max.	Min.	Typ.	Max.
W	15.90	16.00	16.10	0.626	0.630	0.634
E	1.65	1.75	1.85	0.065	0.069	0.073
F	7.40	7.50	7.60	0.291	0.295	0.299
D0	1.40	1.50	1.60	0.055	0.059	0.063
D1	1.40	1.50	1.60	0.055	0.059	0.063
P0	3.90	4.00	4.10	0.154	0.157	0.161
P1	7.90	8.00	8.10	0.311	0.315	0.319
P2	1.90	2.00	2.10	0.075	0.079	0.083
A0	6.85	6.90	7.00	0.270	0.271	0.276
B0	10.45	10.50	10.60	0.411	0.413	0.417
K0	2.68	2.78	2.88	0.105	0.109	0.113
T	0.24			0.27	0.009	
t1	0.10			0.004		
10P0	39.80	40.00	40.20	1.567	1.575	1.583