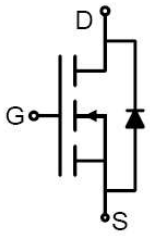
Feature

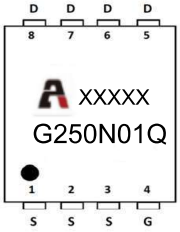
- 100V,25A
  $R_{DS(ON)}$ <25mΩ @V_{GS}=10V (TYP:20mΩ)
  $R_{DS(ON)}$ <38mΩ @V_{GS}=4.5V (TYP:30 mΩ)
- Split Gate Trench Technology
- Lead free product is acquired
- Excellent $R_{DS(ON)}$ and Low Gate Charge



Schematic Diagram

Application

- PWM applications
- Load Switch
- Power management



Marking and pin Assignment

Package Marking and Ordering Information

Device Marking	Device	Device Package	Reel Size	Tape width	Quantity (PCS)
G250N01Q	APG250N01Q	PDFN3*3-8L	13 Inch	-	5000

ABSOLUTE MAXIMUM RATINGS (T_a=25℃ unless otherwise noted)

Parameter	Symbol	Value	Unit
Drain-Source Voltage	V_{DS}	100	V
Gate-Source Voltage	V_{GS}	±20	V
Continuous Drain Current (T_a =25℃)	I_D	25	A
Continuous Drain Current (T_a =100℃)	I_D	18	A
Pulsed Drain Currenr (1)	I_{DM}	100	A
Singel Pulsed Avalanche Energy (2)	E_{AS}	16	mJ
Power Dissipation	P_D	45	W
Thermal Resistance from Junction to Case	$R_{\theta JC}$	2.5	℃/W
Junction Temperature	T_J	150	℃
Storage Temperature	T_{STG}	-55~ +150	℃

MOSFET ELECTRICAL CHARACTERISTICS(T_a=25℃ unless otherwise noted)

Parameter	Symbol	Test Condition	Min	Type	Max	Unit
Static Characteristics						
Drain-source breakdown voltage	$V_{(BR)DSS}$	V_{GS} = 0V, I_D =250μA	100	-	-	V
Zero gate voltage drain current	I_{DSS}	V_{DS} =100V, V_{GS} = 0V	-	-	1	μA
Gate-body leakage current	I_{GSS}	V_{GS} =±20V, V_{DS} = 0V	-	-	±100	nA
Gate threshold voltage(3)	$V_{GS(th)}$	V_{DS} =V_{GS}, I_D =250μA	1.2	1.8	2.8	V
Drain-source on-resistance(3)	$R_{DS(on)}$	V_{GS} =10V, I_D =15A	-	20	25	mΩ
		V_{GS} =4.5V, I_D =10A	-	30	38	mΩ
Forward Threshold Voltage	g_{fs}	V_{DS} =10V, I_D =20A	-	22	-	S
Gate Resistance	R_g	V_{DS} =V_{GS} =0V, f =1MHz	-	1.62	-	Ω
Dynamic characteristics						
Input Capacitance	C_{iss}	V_{DS} =50V, V_{GS} =0V, f =1MHz	-	822	-	pF
Output Capacitance	C_{oss}		-	310	-	
Reverse Transfer Capacitance	C_{rss}		-	23.5	-	
Switching characteristics						
Turn-on delay time	$t_{d(on)}$	V_{DD}=50V, I_D=20A, V_{GS}=10V, R_G=3Ω	-	15	-	ns
Turn-on rise time	t_r		-	3.2	-	
Turn-off delay time	$t_{d(off)}$		-	30	-	
Turn-off fall time	t_f		-	7.6	-	
Total Gate Charge	Qg	VDS=50V, ID=20A, VGS=10V	-	22.7	-	nC
Gate-Source Charge	Qgs		-	6.2	-	
Gate-Drain Charge	Qgd		-	5.3	-	
Reverse Recovery Chrage	Qrr	I_F=20A,di/dt=100A/us		59		nC
Reverse Recovery Time	Trr	I_F=20A,di/dt=100A/us		45		ns
Source-Drain Diode characteristics						
Diode Forward voltage(3)	V_{DS}	V_{GS} =0V, I_S=10A	-	-	1.2	V
Diode Forward current(4)	I_S		-	-	25	A

Notes:

1. Repetitive Rating: pulse width limited by maximum junction temperature
2. EAS Condition:T_J=25℃,V_{DD}=50V,R_G=25Ω,L=0.5Mh
3. Pulse Test: pulse width≤300μs, duty cycle≤2%
4. Surface Mounted on FR4 Board,t≤10 sec

Typical Performance Characteristics

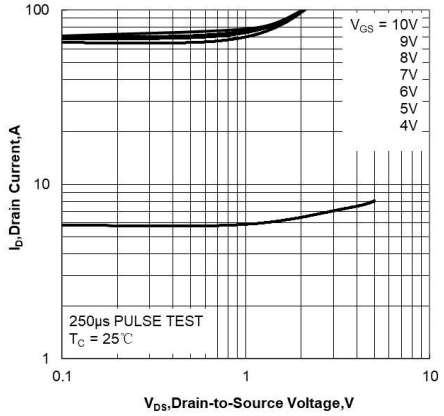


Figure 1. Output Characteristics

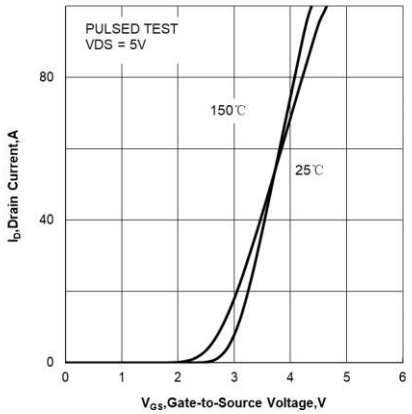


Figure 2. Transfer Characteristics

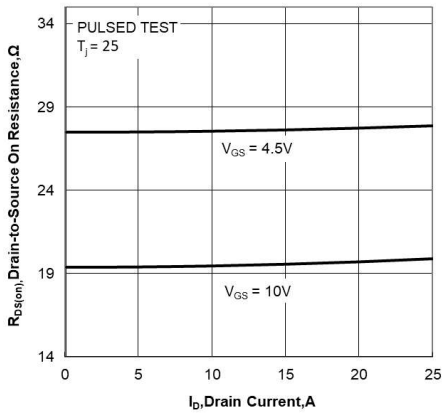


Figure 3. Drain-to-Source On Resistance vs Drain Current

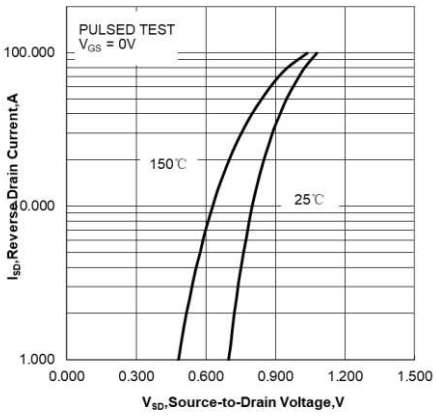


Figure 4. Body Diode Forward Voltage vs Source Current and Temperature

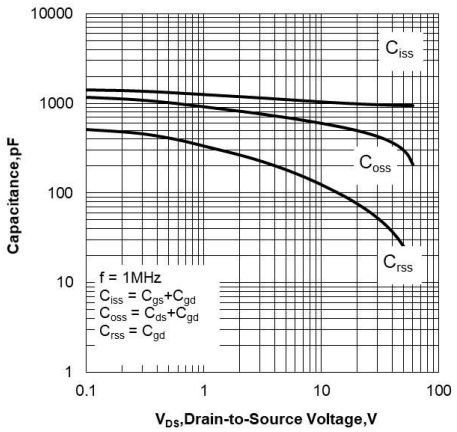


Figure 5. Capacitance Characteristics

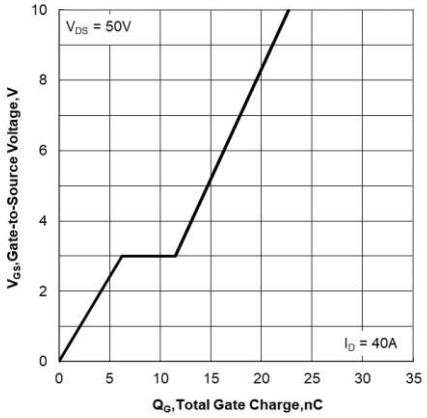


Figure 6. Gate Charge Characteristics

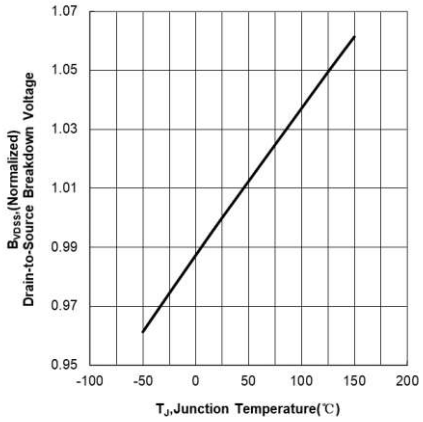


Figure 7. Normalized Breakdown Voltage vs Junction Temperature

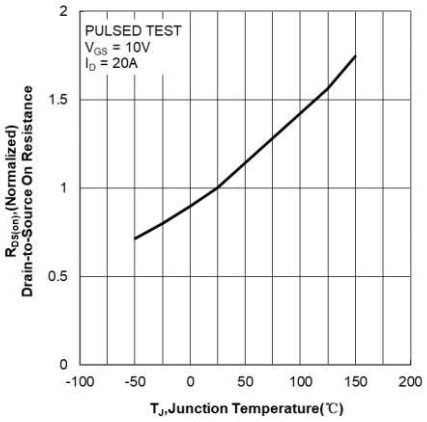


Figure 8. Normalized On Resistance vs Junction Temperature

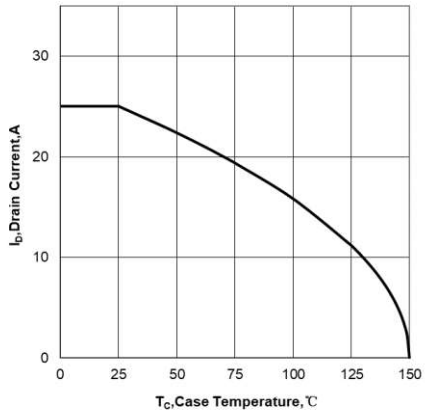


Figure 9. Maximum Continuous Drain Current vs Case Temperature

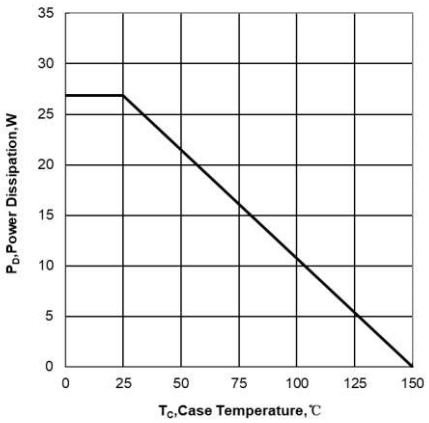


Figure 10. Maximum Power Dissipation vs Case Temperature

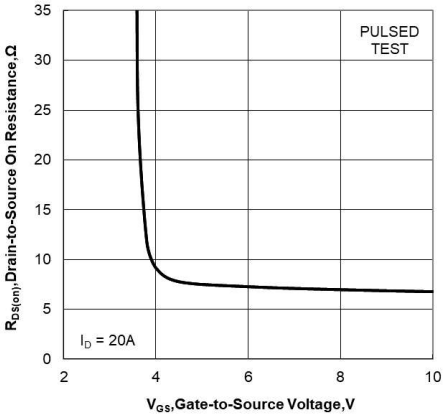


Figure11. Drain-to-Source On Resistance vs Gate Voltage and Drain Current

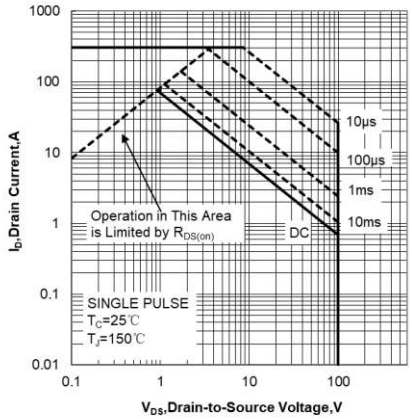


Figure 12. Maximum Safe Operating Area

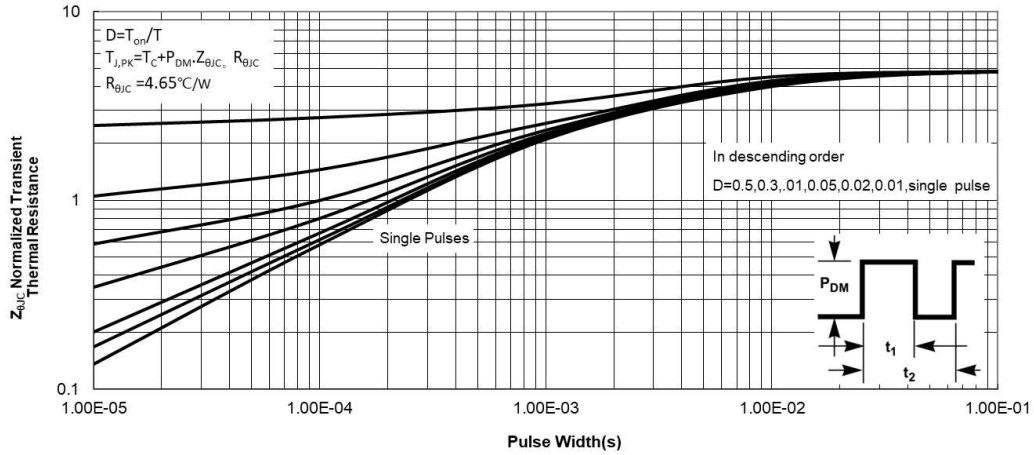
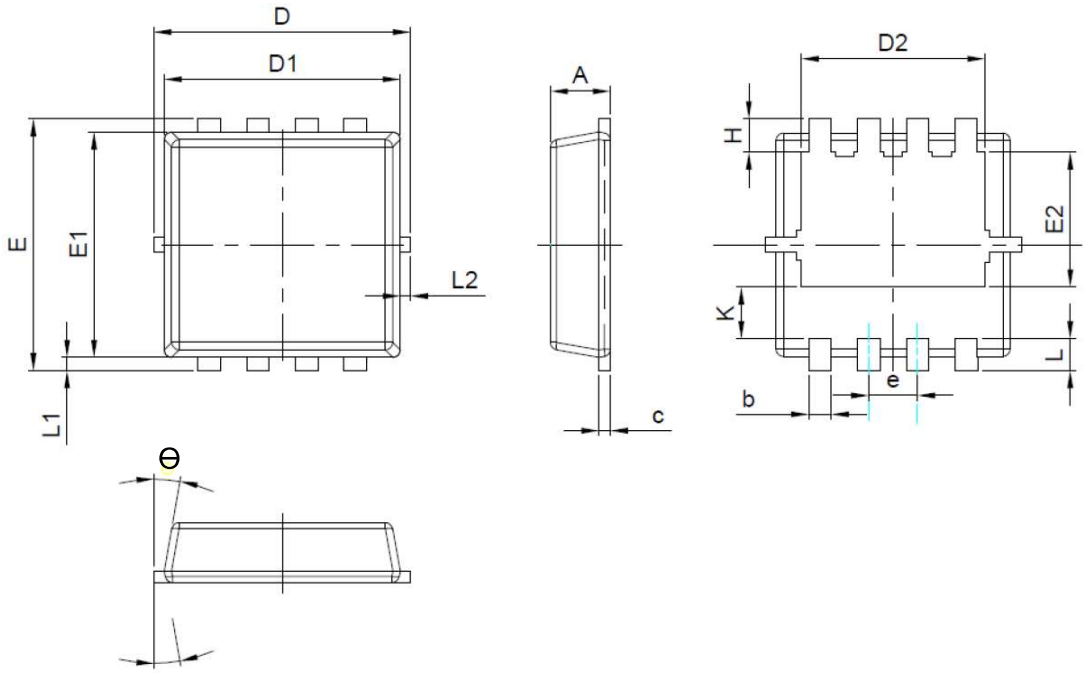


Figure 13. Maximum Effective Transient Thermal Impedance, Junction-to-Case

PDFN3X3-8L Package Information



COMMON DIMENSIONS
(UNITS OF MEASURE = MILLIMETER)

SYMBOL	MIN	NOM	MAX
A	0.70	0.80	0.90
b	0.25	0.30	0.39
c	0.14	0.15	0.25
D	3.20	3.30	3.40
D1	3.00	3.15	3.30
D2	2.35	2.45	2.55
e	0.65 BSC		
E	3.25	3.35	3.45
E1	2.85	3.00	3.15
E2	1.635	1.735	1.835
H	0.33	0.48	0.63
K	0.585	0.685	0.785
L	0.30	0.40	0.50
L1	0.05	0.15	0.25
L2	-	-	0.15
Θ	8°	10°	12°