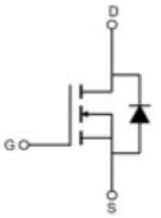
AP3010

N-Channel Enhancement Mosfet

DATA SHEET

Feature

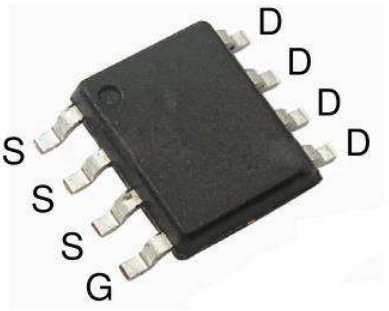
- 30V,10A
  $R_{DS(ON)}$ <10mΩ @V_{GS}=10V TYP:8.5mΩ
  $R_{DS(ON)}$ <14mΩ @V_{GS}=4.5V TYP:11 mΩ
- Advanced Trench Technology
- Lead free product is acquired
- Excellent $R_{DS(ON)}$ and Low Gate Charge



Schematic Diagram

Application

- PWM applications
- Load Switch
- Power management



SOP-8

Package Marking and Ordering Information

Device Marking	Device	Device Package	Reel Size	Tape width	Quantity (PCS)
3010	AP3010	SOP-8	13 inch	-	4000

ABSOLUTE MAXIMUM RATINGS (T_a=25℃ unless otherwise noted)

Parameter	Symbol	Value	Unit
Drain-Source Voltage	V_{DS}	30	V
Gate-Source Voltage	V_{GS}	±20	V
Continuous Drain Current (T_a =25℃)	I_D	10	A
Continuous Drain Current (T_a =100℃)	I_D	6	A
Pulsed Drain Currenr (1)	I_{DM}	50	A
Singel Pulsed Avalanche Energy (2)	E_{AS}	45	mJ
Power Dissipation	P_D	2.5	W
Thermal Resistance from Junction to Case(4)	$R_{\theta JC}$	50	℃/W
Junction Temperature	T_J	150	℃
Storage Temperature	T_{STG}	-55~ +150	℃

MOSFET ELECTRICAL CHARACTERISTICS(T_a=25℃ unless otherwise noted)

Parameter	Symbol	Test Condition	Min	Type	Max	Unit
Static Characteristics						
Drain-source breakdown voltage	$V_{(BR)DSS}$	V_{GS} = 0V, I_D =250μA	30	-	-	V
Zero gate voltage drain current	I_{DSS}	V_{DS} =30V, V_{GS} = 0V	-	-	1	μA
Gate-body leakage current	I_{GSS}	V_{GS} =±20V,V_{DS} = 0V	-	-	±100	nA
Gate threshold voltage(3)	$V_{GS(th)}$	V_{DS} =V_{GS}, I_D =250μA	1	1.6	2.5	V
Drain-source on-resistance(3)	$R_{DS(on)}$	V_{GS} =10V, I_D =10A	-	8.5	10	mΩ
		V_{GS} =4.5V, I_D =5A	-	11	14	
Dynamic characteristics						
Input Capacitance	C_{iss}	V_{DS} =15V, V_{GS} =0V, f =1MHz	-	900	-	pF
Output Capacitance	C_{oss}		-	140	-	
Reverse Transfer Capacitance	C_{rss}		-	120	-	
Switching characteristics						
Turn-on delay time	$t_{d(on)}$	V_{DD}=15V, I_D=10A, R_L=6Ω V_{GS}=10V, R_G=1Ω	-	6	-	ns
Turn-on rise time	t_r		-	5	-	
Turn-off delay time	$t_{d(off)}$		-	25	-	
Turn-off fall time	t_f		-	7	-	
Total Gate Charge	Qg	VDS=15V, ID=10A, VGS=10V	-	19	-	nC
Gate-Source Charge	Qgs		-	6.3	-	
Gate-Drain Charge	Qgd		-	4.5	-	
Source-Drain Diode characteristics						
Diode Forward voltage(3)	V_{DS}	V_{GS} =0V, I_S=10A	-	-	1.2	V
Diode Forward current(4)	I_S		-	-	10	A

Notes:

1. Repetitive Rating: pulse width limited by maximum junction temperature
2. EAS Condition:T_J=25℃,V_{DD}=15V,R_G=25Ω,L=0.5mH
3. Pulse Test: pulse width≤300μs, duty cycle≤2%
4. Surface Mounted on FR4 Board,t≤10 sec

Test Circuit

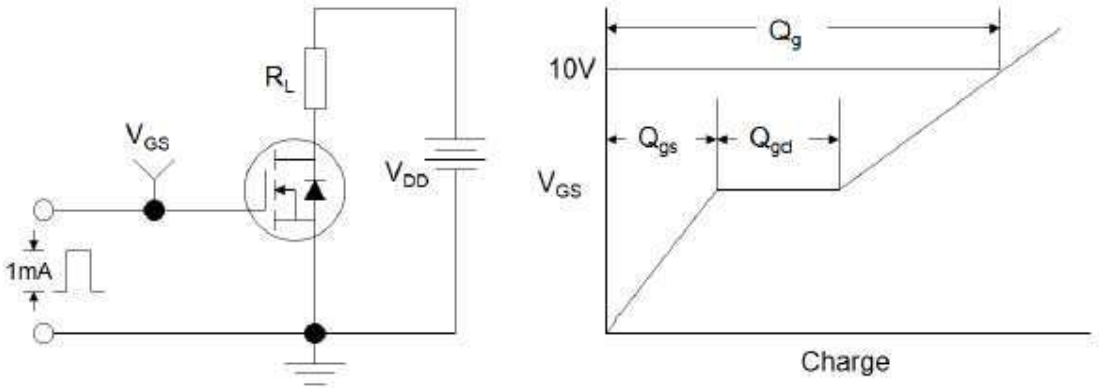


Figure1:Gate Charge Test Circuit & Waveform

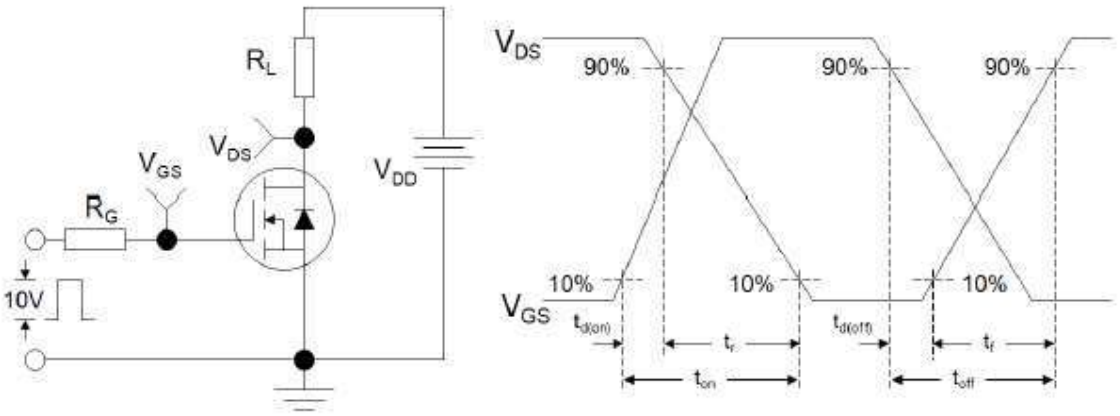


Figure 2: Resistive Switching Test Circuit & Waveforms

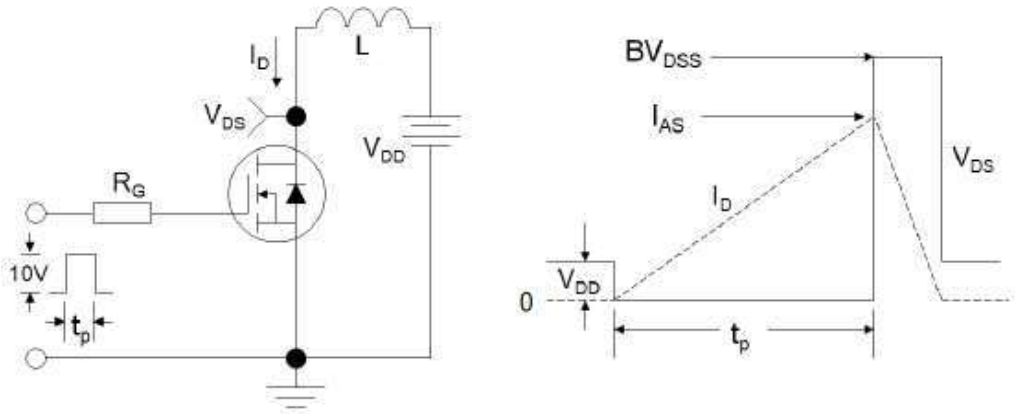


Figure 3:Unclamped Inductive Switching Test Circuit & Waveforms

Typical Performance Characteristics

Figure1: Output Characteristics

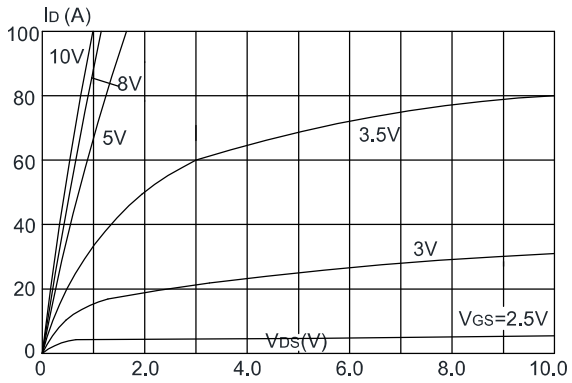


Figure 2: Typical Transfer Characteristics

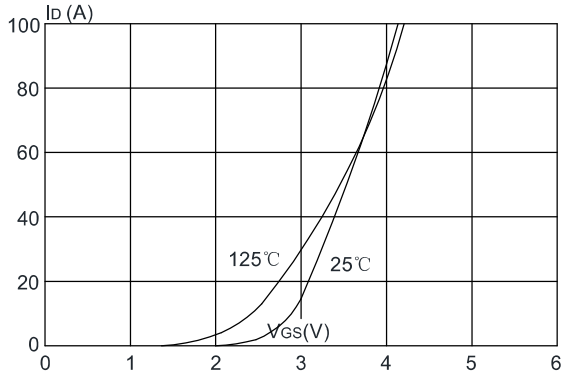


Figure 3: On-resistance vs. Drain Current

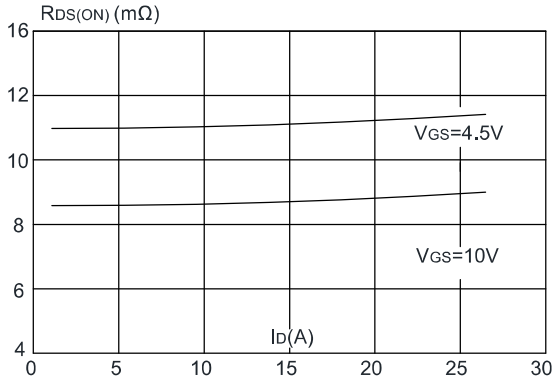


Figure 4: Body Diode Characteristics

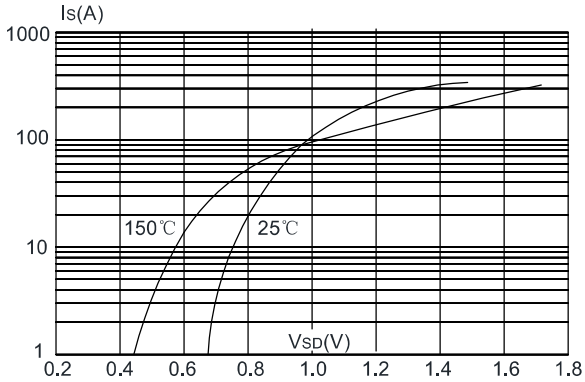


Figure 5: Gate Charge Characteristics

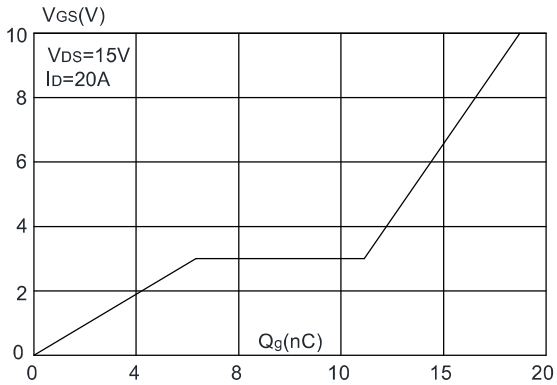


Figure 6: Capacitance Characteristics

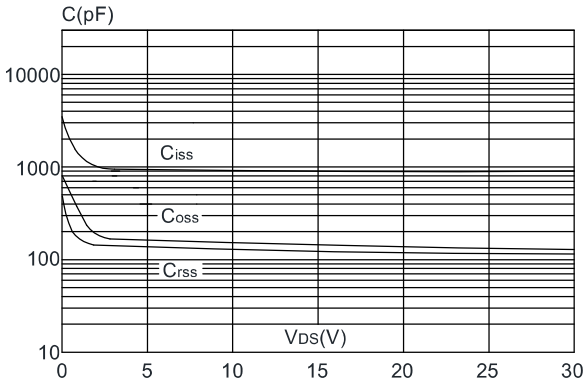


Figure 7: Normalized Breakdown Voltage vs. Junction Temperature

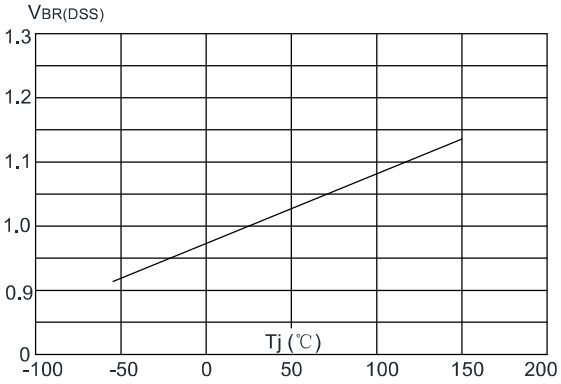


Figure 8: Normalized on Resistance vs. Junction Temperature

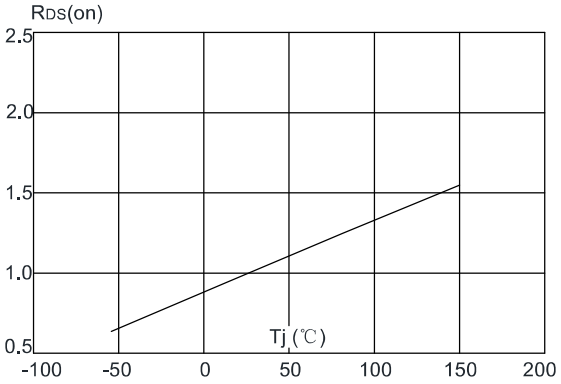


Figure 9: Maximum Safe Operating Area

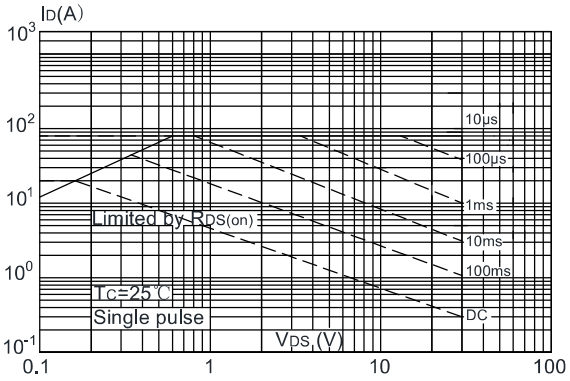


Figure 10: Maximum Continuous Drain Current vs. Case Temperature

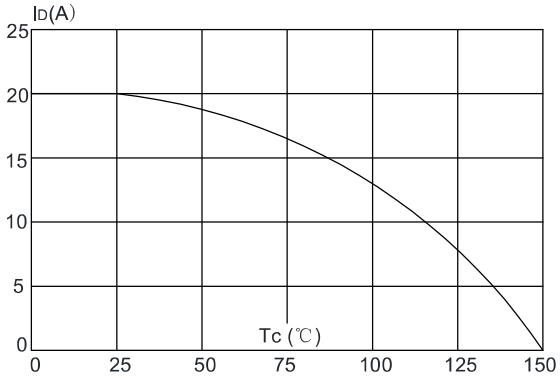
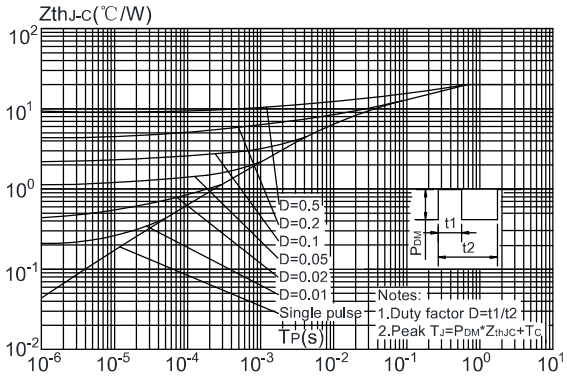
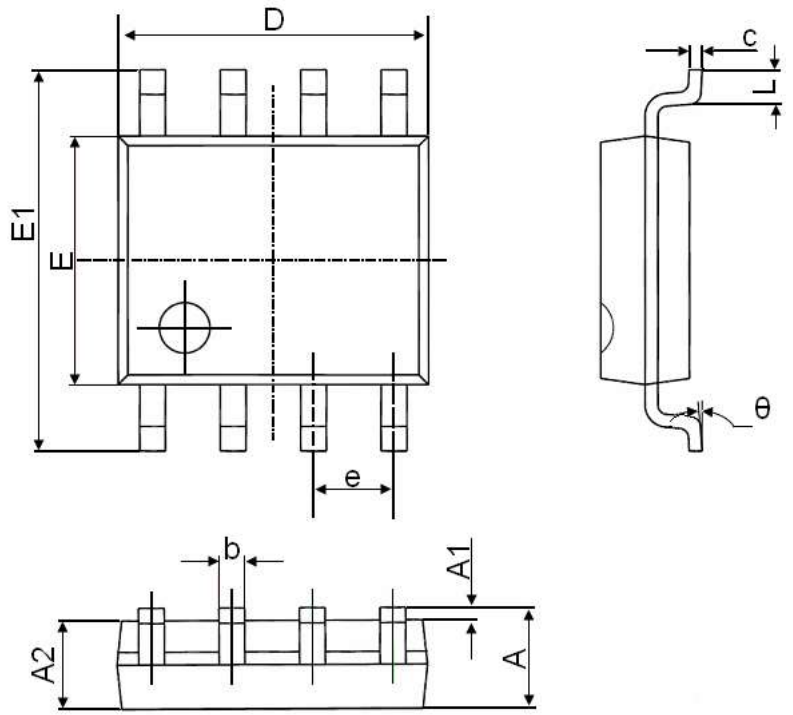


Figure.11: Maximum Effective Transient Thermal Impedance, Junction-to-Case



SOP-8 Package Information



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min.	Max.	Min.	Max.
A	1.350	1.750	0.053	0.069
A1	0.100	0.250	0.004	0.010
A2	1.350	1.550	0.053	0.061
b	0.330	0.510	0.013	0.020
c	0.170	0.250	0.006	0.010
D	4.700	5.100	0.185	0.200
E	3.800	4.000	0.150	0.157
E1	5.800	6.200	0.228	0.244
e	1.270(BSC)		0.050(BSC)	
L	0.400	1.270	0.016	0.050
θ	0°	8°	0°	8°