

# AP8N80

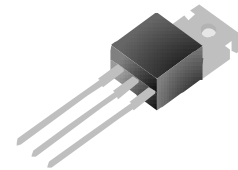
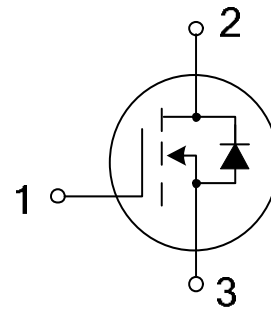
## N-Channel Enhancement Mosfet

# AIPOWER

## DATA SHEET

### Features

- 800V,8A  
 $R_{DS(ON)} < 1.55 \Omega @ V_{GS}=10V$  TYP:1.42  $\Omega$
- Low gate charge
- Low Crss
- Fast switching
- Improved dv/dt capability



TO-220

### Applications

- AC-DC power suppliers,
- DC-DC converters
- H-bridge PWM motor drivers

### Package Marking and Ordering Information

Device Marking	Device	Device Package	Reel Size	Tape width	Quantity (PCS)
8N80	AP8N80	TO-220	-	-	1000

### ABSOLUTE MAXIMUM RATINGS ( $T_a=25^\circ\text{C}$ unless otherwise noted)

Parameter	Symbol	Value	Unit
Drain-Source Voltage	$V_{DS}$	800	V
Gate-Source Voltage	$V_{GS}$	$\pm 30$	V
Continuous Drain Current ( $T_c = 25^\circ\text{C}$ )	$I_D$	8	A
Continuous Drain Current ( $T_c = 100^\circ\text{C}$ )	$I_D$	5.1	A
Pulsed Source Current <sup>(1)</sup>	$I_{sm}$	32	A
Pulsed Drain Current <sup>(1)</sup>	$I_{DM}$	32	A
Single Pulsed Avalanche Energy <sup>(2)</sup>	$E_{AS}$	534	mJ
Power Dissipation	$P_D$	178	W
Thermal Resistance from Junction to Case	$R_{\theta JC}$	0.70	$^\circ\text{C/W}$
Thermal Resistance from Junction to Ambient	$R_{\theta JA}$	62.5	$^\circ\text{C/W}$
Junction Temperature	$T_J$	150	$^\circ\text{C}$
Storage Temperature	$T_{STG}$	-55~ +150	$^\circ\text{C}$

MOSFET ELECTRICAL CHARACTERISTICS( $T_a=25^\circ\text{C}$  unless otherwise noted)

Parameter	Symbol	Test Condition	Min	Type	Max	Unit
<b>Static Characteristics</b>						
Drain-source breakdown voltage	$V_{(BR)DSS}$	$V_{GS} = 0V, I_D = 250\mu A$	800	-	-	V
Zero gate voltage drain current	$I_{DSS}$	$V_{DS} = 800V, V_{GS} = 0V, T_J = 25^\circ\text{C}$	-	-	1	$\mu A$
Gate-body leakage current	$I_{GSS}$	$V_{GS} = \pm 30V, V_{DS} = 0V$	-	-	$\pm 100$	nA
Gate threshold voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}, I_D = 250\mu A$	2.0	-	4.0	V
Drain-source on-resistance <sup>(3)</sup>	$R_{DS(on)}$	$V_{GS} = 10V, I_D = 4A$	-	1.42	1.55	$\Omega$
<b>Dynamic characteristics</b>						
Input Capacitance	$C_{iss}$	$V_{DS} = 25V, V_{GS} = 0V, f = 1.0\text{MHz}$	-	1083	-	pF
Output Capacitance	$C_{oss}$		-	103	-	
Reverse Transfer Capacitance	$C_{rss}$		-	5.8	-	
<b>Switching characteristics</b>						
Turn-on delay time	$t_{d(on)}$	$V_{DD} = 400V, I_D = 8A, R_G = 25\Omega$	-	30.33	-	ns
Turn-on rise time	$t_r$		-	67.0	-	
Turn-off delay time	$t_{d(off)}$		-	58.0	-	
Turn-off fall time	$t_f$		-	38.33	-	
Total Gate Charge	$Q_g$	$V_{DS} = 640V, I_D = 8A, V_{GS} = 10V$	-	24.62	-	nC
Gate-Source Charge	$Q_{gs}$		-	7.26	-	
Gate-Drain Charge	$Q_{gd}$		-	8.97	-	
<b>Source-Drain Diode characteristics</b>						
Diode Forward voltage	$V_{SD}$	$T_J = 25^\circ\text{C}, V_{GS} = 0V, I_S = 8A$	-	-	1.4	V
Diode Forward current	$I_S$	$T_C = 25^\circ\text{C}$	-	-	8.0	A
Body Diode Reverse Recovery Time	$t_{rr}$	$T_J = 25^\circ\text{C}, I_F = 8A, di/dt = 100A/\mu s$		310		ns
Body Diode Reverse Recovery Charge	$Q_{rr}$	$T_J = 25^\circ\text{C}, I_F = 8A, di/dt = 100A/\mu s$		0.53		$\mu c$

**Notes:**

1.  $L=30\text{mH}, I_{AS}=5.50\text{A}, V_{DD}=135\text{V}, R_G=25\Omega$ , starting  $T_J=25^\circ\text{C}$ ;
2. Pulse Test: Pulse width  $\leq 300\mu s$ , Duty cycle  $\leq 2\%$ ;
3. Essentially independent of operating temperature.

**TYPICAL CHARACTERISTICS**

Figure 1. On-Region Characteristics

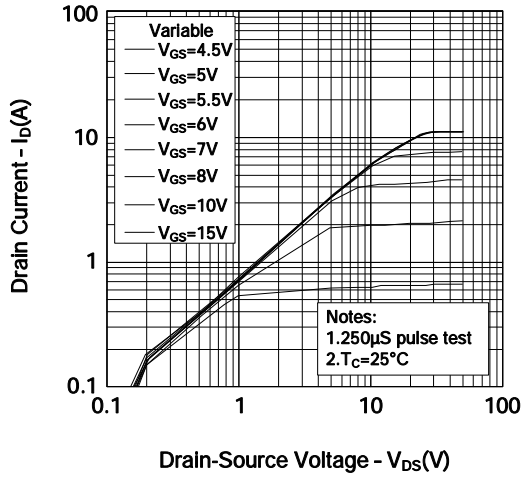


Figure 2. Transfer Characteristics

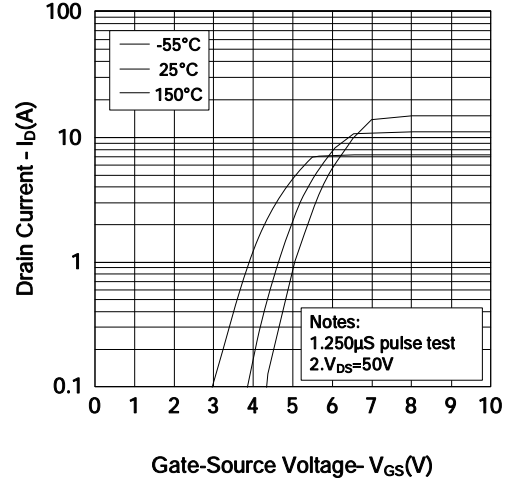


Figure 3. On-Resistance Variation vs. Drain Current and Gate Voltage

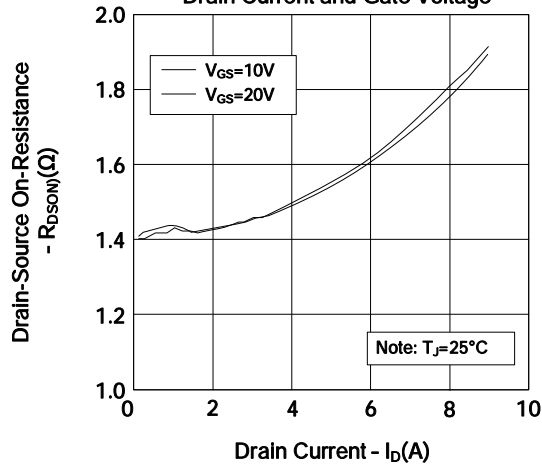


Figure 4. Body Diode Forward Voltage Variation vs. Source Current and Temperature

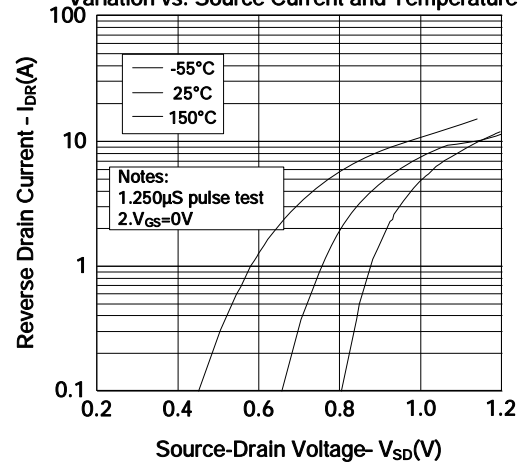


Figure 5. Capacitance Characteristics

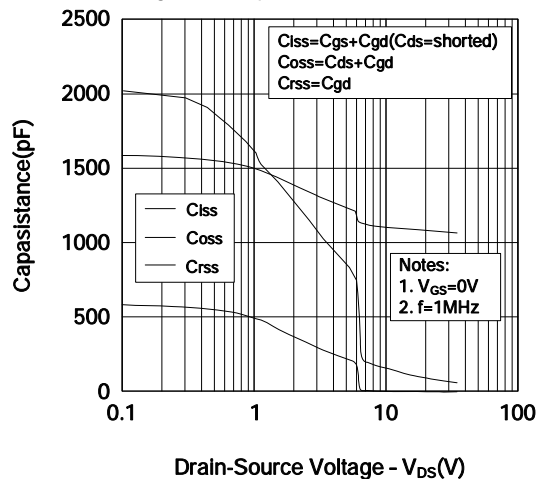
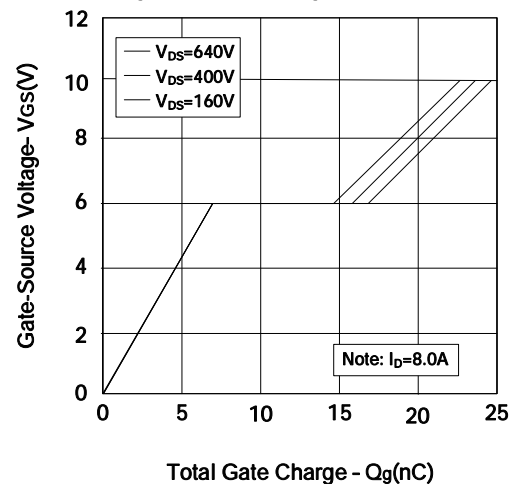


Figure 6. Gate Charge Characteristics



**TYPICAL CHARACTERISTICS(continued)**

Figure 7. Breakdown Voltage Variation vs. Temperature

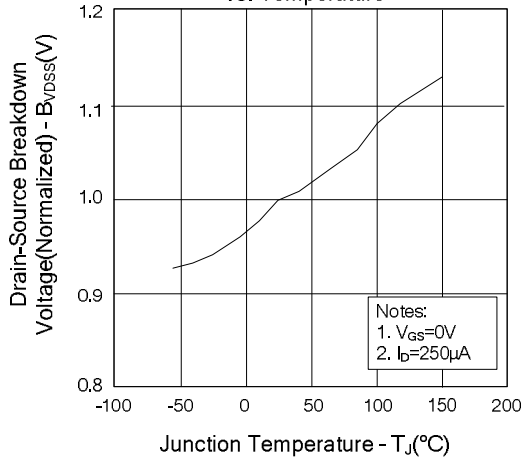


Figure 8. On-resistance Variation vs. Temperature

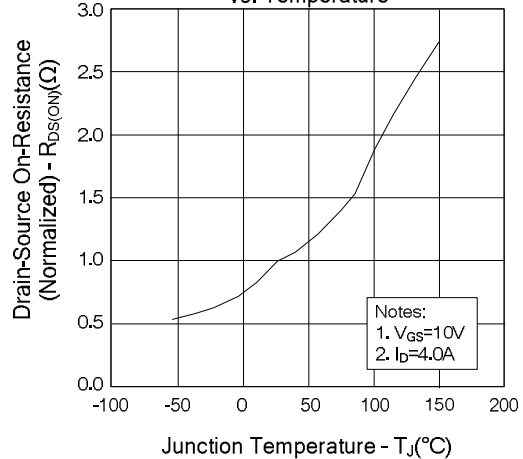


Figure 9-1. Max. Safe Operating Area (SFP8N80)

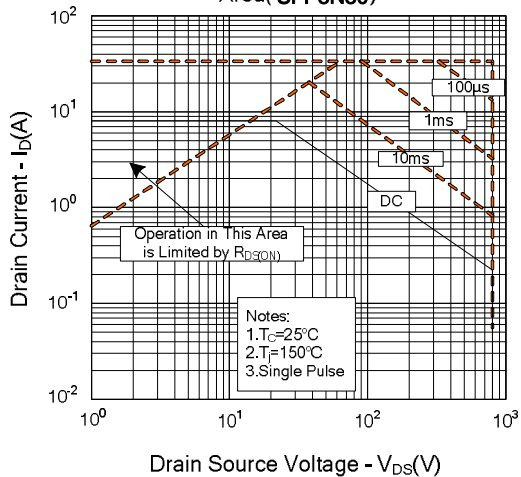


Figure 9-2. Max. Safe Operating Area (SFF8N80)

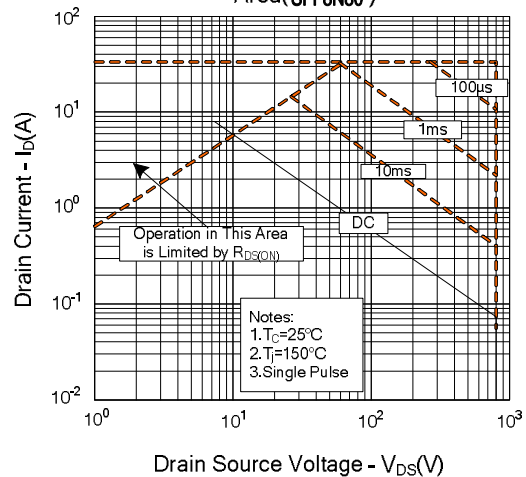
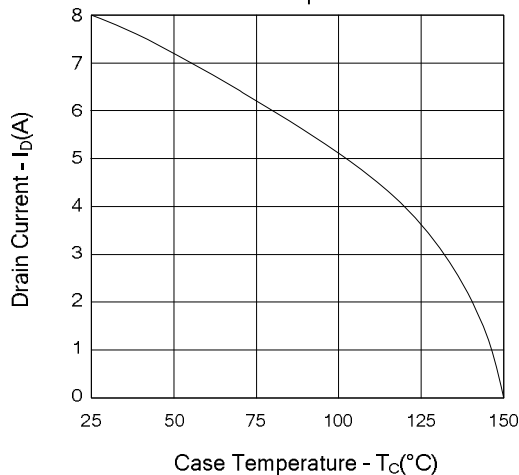
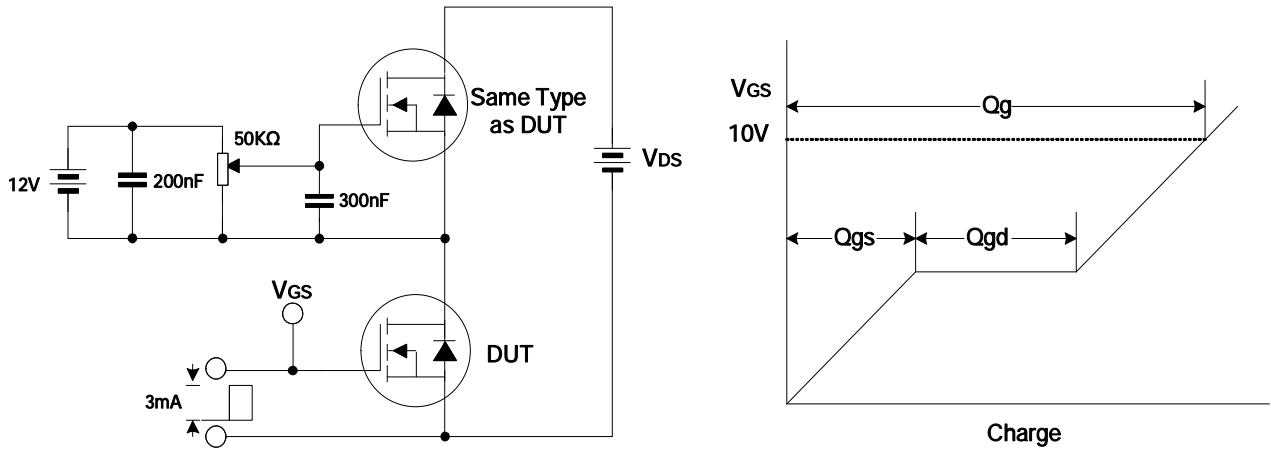


Figure 10. Maximum Drain Current vs. Case Temperature

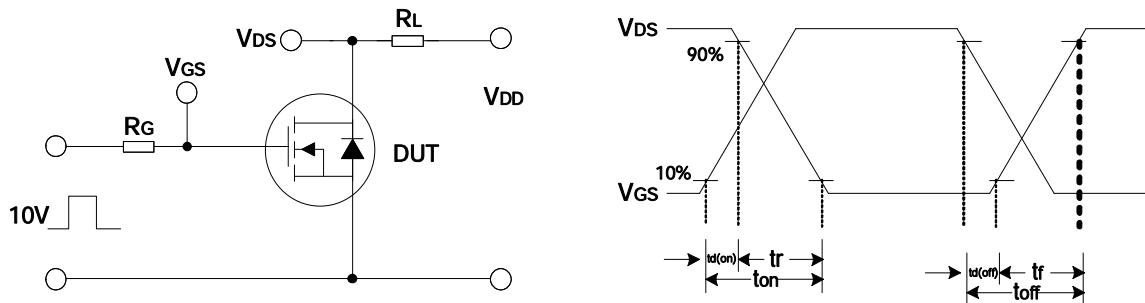


TYPICAL TEST CIRCUIT

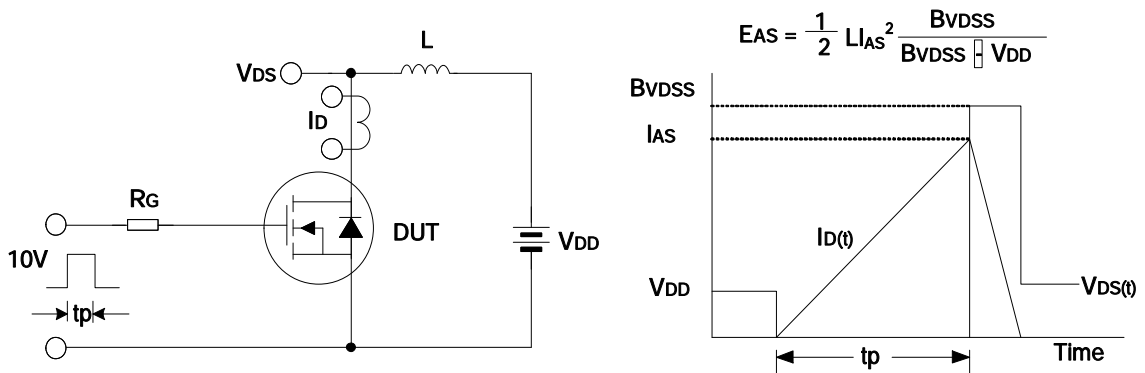
Gate Charge Test Circuit & Waveform



Resistive Switching Test Circuit & Waveform



Unclamped Inductive Switching Test Circuit & Waveform



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PACKAGE OUTLINE(continued)

