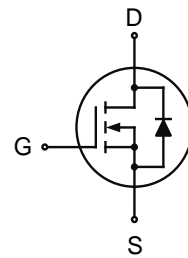


Features

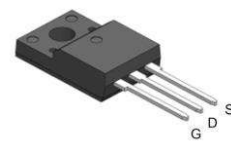
- 650V,7A
 $R_{DS(on)} < 640m\Omega @ V_{GS}=10V$ TYP:523m Ω
- advanced super junction technology
- extremely low on resistance



Schematic Diagram

Applications

- Power faction correction (PFC)
- Switched mode power supplies (SMPS)
- Uninterruptible power supply (UPS)
- LED lighting powe



TO-220F

Package Marking and Ordering Information

Device Marking	Device	Device Package	Reel Size	Tape width	Quantity (PCS)
A65R640FM	APA65R640FM	TO-220F	-	-	1000

ABSOLUTE MAXIMUM RATINGS ($T_a=25^{\circ}C$ unless otherwise noted)

Parameter	Symbol	Value	Unit
Drain-Source Voltage	V_{DS}	650	V
Gate-Source Voltage	V_{GS}	± 30	V
Continuous Drain Current ($T_c = 25^{\circ}C$)	I_D	7	A
Continuous Drain Current ($T_c = 100^{\circ}C$)	I_D	4.4	A
Pulsed Drain Current ⁽¹⁾	I_{DM}	28	A
Single Pulsed Avalanche Energy ⁽²⁾	E_{AS}	249	mJ
Drain Power Dissipation	P_D	35	W
Thermal Resistance from Junction to Case	$R_{\theta JC}$	2.08	$^{\circ}C/W$
Thermal Resistance- Junction to Ambient	$R_{\theta JA}$	62.0	$^{\circ}C/W$
Junction Temperature	T_J	150	$^{\circ}C$
Storage Temperature	T_{STG}	-55~ +150	$^{\circ}C$
Maximum Lead temperature for soldering Purpose	T_L	300	$^{\circ}C$

MOSFET ELECTRICAL CHARACTERISTICS(T_a=25°C unless otherwise noted)

Parameter	Symbol	Test Condition	Min	Type	Max	Unit
Static Characteristics						
Drain-source breakdown voltage	V _{(BR)DSS}	V _{GS} = 0V, I _D =250μA	650	-	-	V
Zero gate voltage drain current	I _{DSS}	V _{DS} =650V, V _{GS} = 0V	-	-	100	nA
Gate-body leakage current	I _{GSS}	V _{GS} = ±30V, V _{DS} = 0V	-	-	±100	nA
Gate threshold voltage	V _{GS(th)}	V _{DS} =V _{GS} , I _D =250μA	2.0	3.4	4.0	V
Forward Transconductance ⁽³⁾	g _{FS}	V _{DS} =25V, I _D =7A	-	4.9	-	S
Drain-source on-resistance	R _{DS(on)}	V _{GS} =10V, I _D =5.5A	-	523	640	mΩ
Dynamic characteristics						
Input Capacitance	C _{iss}	V _{DS} =100V, V _{GS} =0V, f =1.0MHz	-	423	-	pF
Output Capacitance	C _{oss}		-	26	-	
Reverse Transfer Capacitance	C _{rss}		-	1.7	-	
Switching characteristics ^(3,4)						
Turn-on delay time	t _{d(on)}	V _{DD} =325V, I _D =7A, R _G =24Ω, V _G =10V	-	11.2	-	ns
Turn-on rise time	t _r		-	28.6	-	
Turn-off delay time	t _{d(off)}		-	46.7	-	
Turn-off fall time	t _f		-	24.4	-	
Total Gate Charge	Q _g	V _{DS} =520V, I _D =7A, V _{GS} =10V	-	16.4	-	nC
Gate-Source Charge	Q _{gs}		-	3.5	-	
Gate-Drain Charge	Q _{gd}		-	8.3	-	
Source-Drain Diode characteristics						
Diode Forward voltage	V _{SD}	T _c =25°C, V _{GS} =0V, I _S =7A	-	0.87	1.4	V
Diode Forward current	I _S	T _c =25°C	-	-	11	A
Body Diode Reverse Recovery Time ⁽³⁾	t _{rr}	T _c =25°C, I _F =7A, di/dt=100A/us		340		ns
Body Diode Reverse Recovery Charge	Q _{rr}	T _c =25°C, I _F =7A, di/dt=100A/us		2.5		uc

Notes:

1. Pulse width limited by maximum junction temperature
2. L=79mH, I_{AS}=2.2A, V_{DD}=100V, V_G=10V, R_G=25Ω, starting T_J=25°C
3. Pulse Test: Pulse width ≤300μs, Duty cycle≤2%
4. Essentially independent of operating temperature

Typical Performance Characteristics

Figure 1. On-Region Characteristics

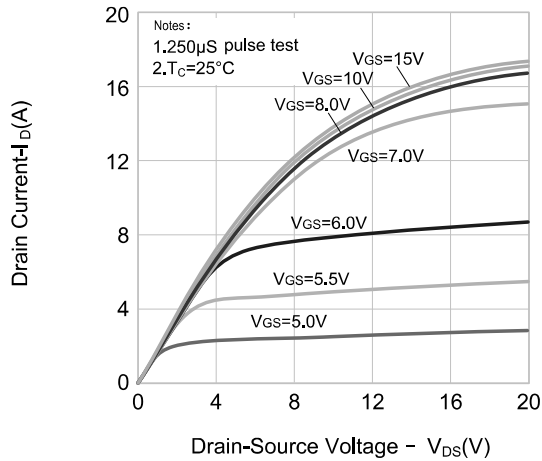


Figure 2. Transfer Characteristics

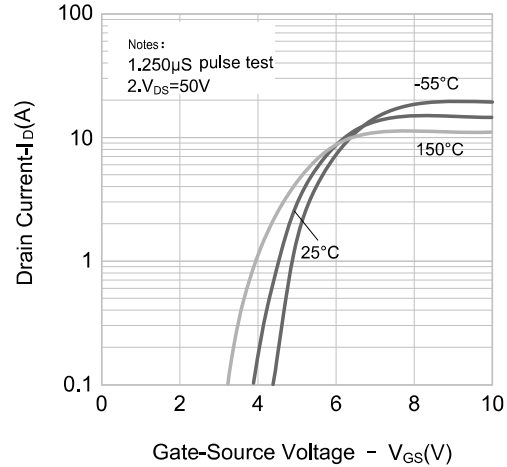


Figure 3. On-Resistance Variation vs. Drain-Current, Gate Voltage

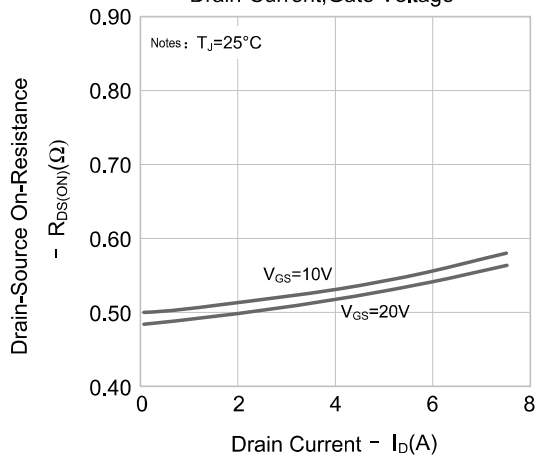


Figure 4. Body Diode Forward Voltage Variation vs. Source Current and Temperature

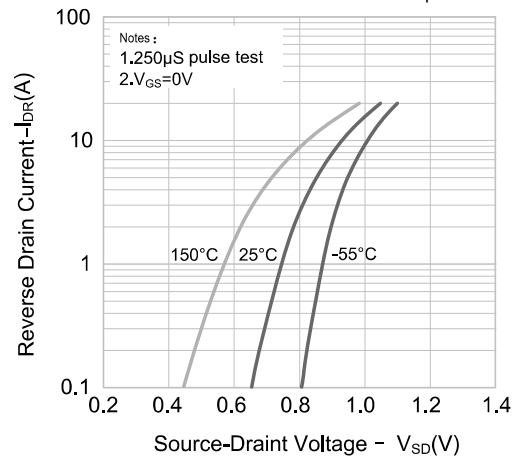


Figure 5. Capacitance Characteristics

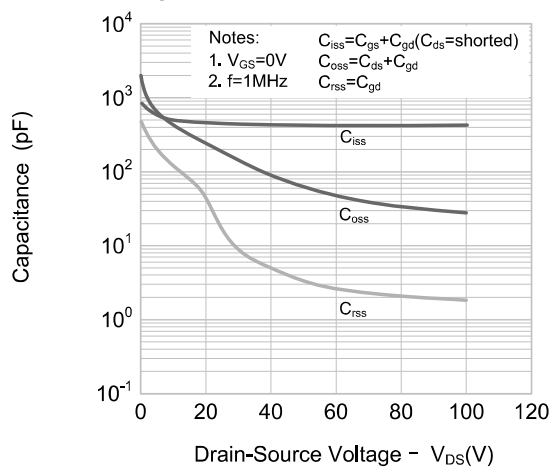
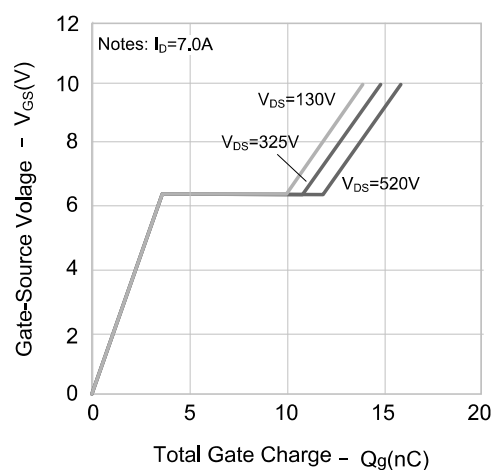


Figure 6. Gate Charge Characteristics



Typical Performance Characteristics

Figure 7. Breakdown Voltage Variation vs. Temperature

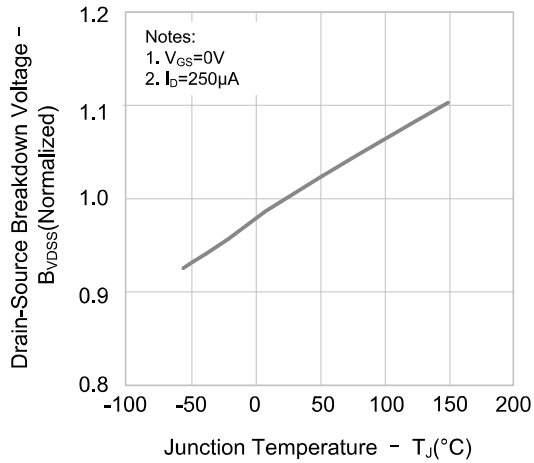


Figure 8. On-resistance Variation vs. Temperature

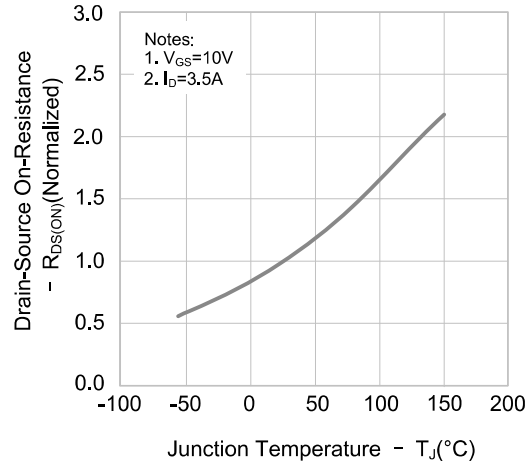


Figure 9.1 Max. Safe Operating Area (SCD65R640C)

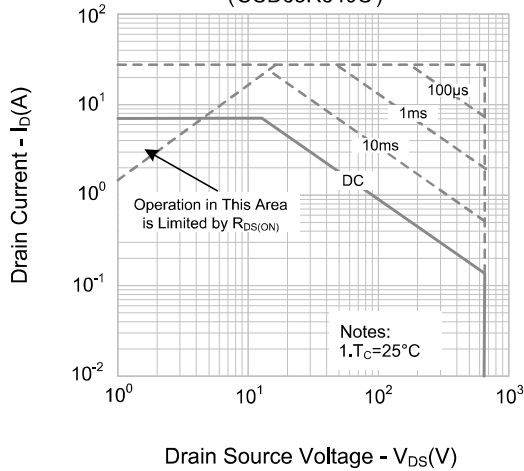
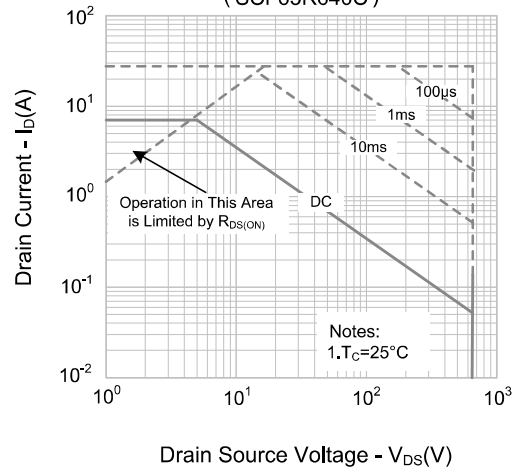
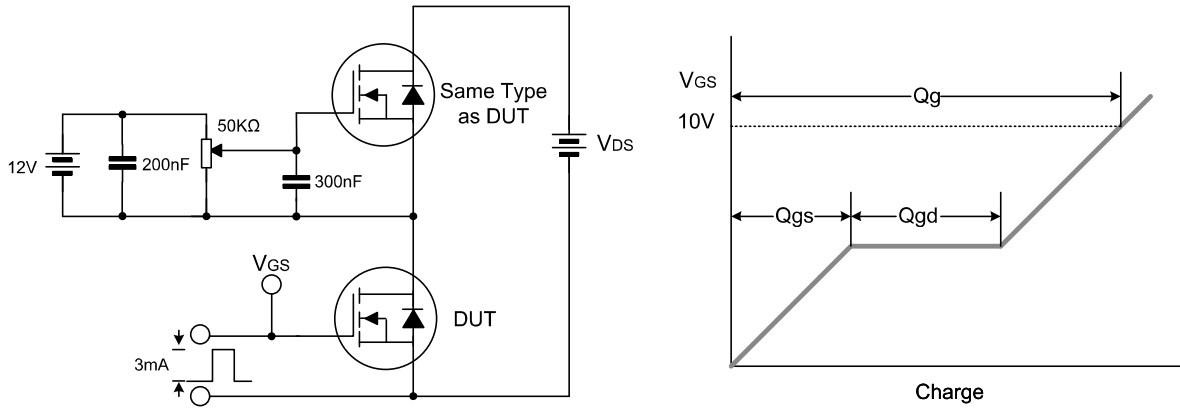


Figure 9.2 Max. Safe Operating Area (SCF65R640C)

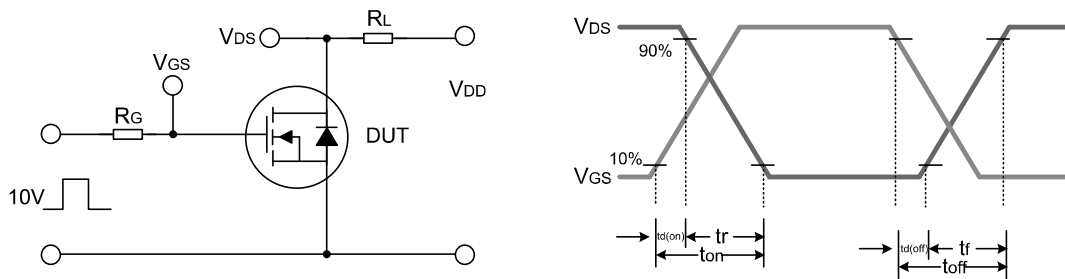


Test Circuit

Gate Charge Test Circuit & Waveform



Resistive Switching Test Circuit & Waveform



Unclamped Inductive Switching Test Circuit & Waveform

