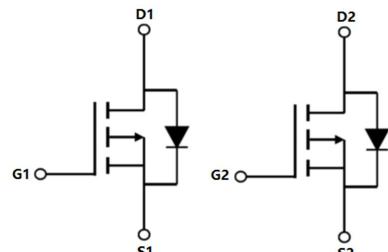


Feature

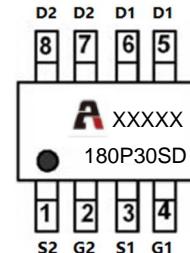
- -30V,-9A
 $R_{DS(ON)} < 23m\Omega @ V_{GS} = -10V$
 $R_{DS(ON)} < 32m\Omega @ V_{GS} = -4.5V$
- Trench DMOS Power MOSFET
- Fast Switching
- Exceptional on-resistance and maximum DC current capability



Schematic Diagram

Application

- DC/DC Converter
- Load Switch for Portable Devices
- Battery Switch



Marking and pin Assignment

Package Marking and Ordering Information

Device Marking	Device	Device Package	Reel Size	Tape width	Quantity (PCS)
180P30SD	AP180P30SD	SOP-8	13 inch	-	4000

ABSOLUTE MAXIMUM RATINGS ($T_J=25^\circ C$ unless otherwise noted)

Parameter	Symbol	Value	Unit
Drain-Source Voltage	V_{DS}	-30	V
Gate-Source Voltage	V_{GS}	± 20	V
Continuous Drain Current ($T_a = 25^\circ C$)	I_D	-9	A
Continuous Drain Current ($T_a = 100^\circ C$)	I_D	-5.9	A
Pulsed Drain Current ⁽¹⁾	I_{DM}	-36	A
Single Pulsed Avalanche Energy ⁽⁴⁾	E_{AS}	36	mJ
Power Dissipation ($T_a = 25^\circ C$)	P_D	3.3	W
Thermal Resistance from Junction to Ambient	$R_{\theta JA}$	38	$^\circ C/W$
Junction Temperature	T_J	150	$^\circ C$
Storage Temperature	T_{STG}	-55~+150	$^\circ C$

MOSFET ELECTRICAL CHARACTERISTICS($T_j=25^\circ\text{C}$ unless otherwise noted)

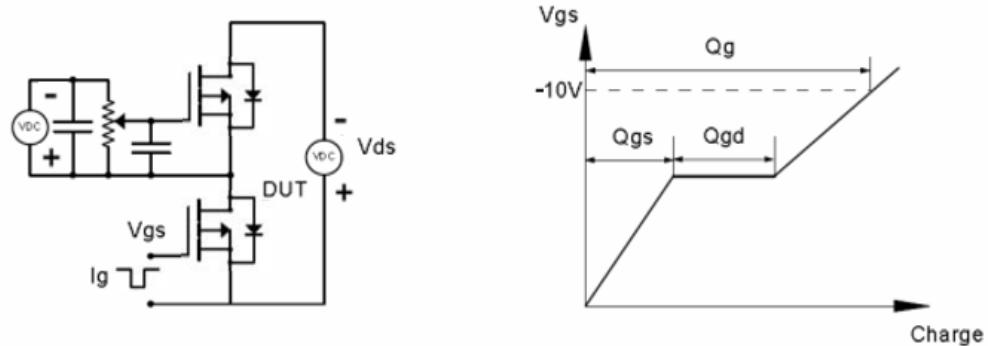
Parameter	Symbol	Test Condition	Min	Type	Max	Unit
Static Characteristics						
Drain-source breakdown voltage	$V_{(\text{BR})\text{DSS}}$	$V_{\text{GS}} = 0\text{V}, I_D = -250\mu\text{A}$	-30	-	-	V
Zero gate voltage drain current	I_{DSS}	$V_{\text{DS}} = -30\text{V}, V_{\text{GS}} = 0\text{V}$	-	-	-1	μA
Gate-body leakage current	I_{GSS}	$V_{\text{GS}} = \pm 20\text{V}, V_{\text{DS}} = 0\text{V}$	-	-	± 100	nA
Gate threshold voltage ⁽²⁾	$V_{\text{GS}(\text{th})}$	$V_{\text{DS}} = V_{\text{GS}}, I_D = -250\mu\text{A}$	-1	-1.5	-2.5	V
Drain-source on-resistance ⁽²⁾	$R_{\text{DS}(\text{on})}$	$V_{\text{GS}} = -10\text{V}, I_D = -9\text{A}$	-	18	23	$\text{m}\Omega$
		$V_{\text{GS}} = -4.5\text{V}, I_D = -9\text{A}$	-	23	32	
Dynamic characteristics						
Input Capacitance	C_{iss}	$V_{\text{DS}} = -15\text{V}, V_{\text{GS}} = 0\text{V}, f = 1\text{MHz}$	-	2180	-	pF
Output Capacitance	C_{oss}		-	260	-	
Reverse Transfer Capacitance	C_{rss}		-	240	-	
Switching characteristics						
Turn-on delay time	$t_{\text{d}(\text{on})}$	$V_{\text{DD}} = -15\text{V}, I_D = -15\text{A}$ $V_{\text{GS}} = -10\text{V}, R_G = 1\Omega$	-	5.6	-	ns
Turn-on rise time	t_r		-	28	-	
Turn-off delay time	$t_{\text{d}(\text{off})}$		-	52	-	
Turn-off fall time	t_f		-	13.6	-	
Total Gate Charge	Q_g	$V_{\text{DS}} = -15\text{V}, I_D = -15\text{A},$ $V_{\text{GS}} = -10\text{V}$	-	42	-	nC
Gate-Source Charge	Q_{gs}		-	6.1	-	
Gate-Drain Charge	Q_{gd}		-	9.2	-	
Source-Drain Diode characteristics						
Diode Forward voltage ⁽²⁾	V_{DS}	$V_{\text{GS}} = 0\text{V}, I_S = -10\text{A}$	-	-	-1.2	V
Diode Forward current ⁽³⁾	I_S		-	-	-10	A

Notes:

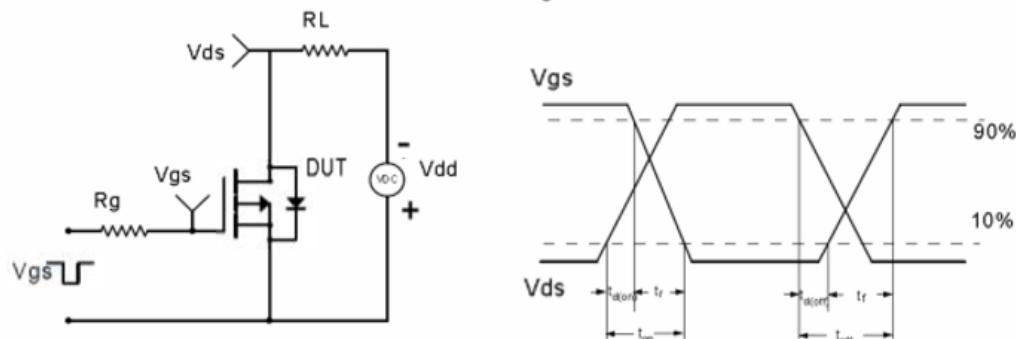
1. Repetitive Rating: pulse width limited by maximum junction temperature
2. Pulse Test: pulse width $\leq 300\mu\text{s}$, duty cycle $\leq 2\%$
3. Surface Mounted on FR4 Board, $t \leq 10$ sec
4. $L = 0.5\text{MH}, V_{\text{DD}} = -15\text{V}, R_G = 25\Omega$, Starting $T_j = 25^\circ\text{C}$

Test Circuit & Waveform

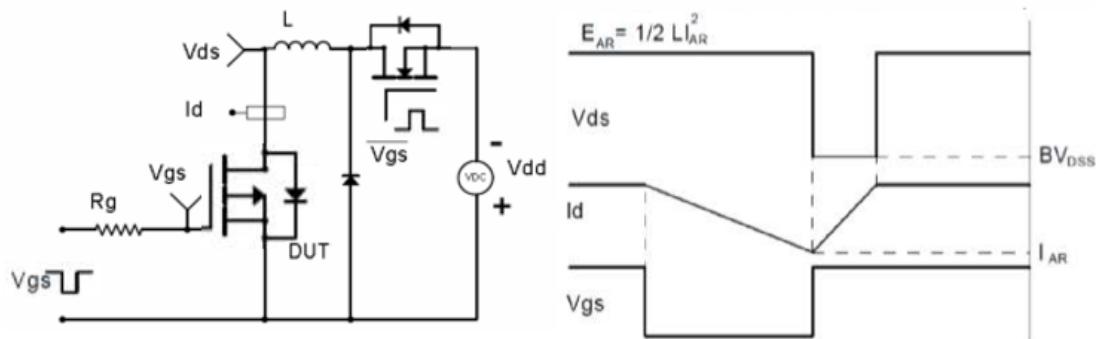
Gate Charge Test Circuit & Waveform



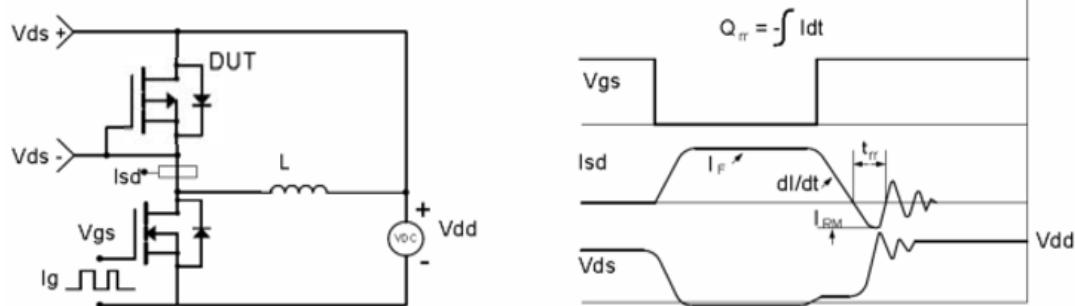
Resistive Switching Test Circuit & Waveforms



Unclamped Inductive Switching (UIS) Test Circuit & Waveforms



Diode Recovery Test Circuit & Waveforms



Typical Performance Characteristics

Figure 1: Output Characteristics

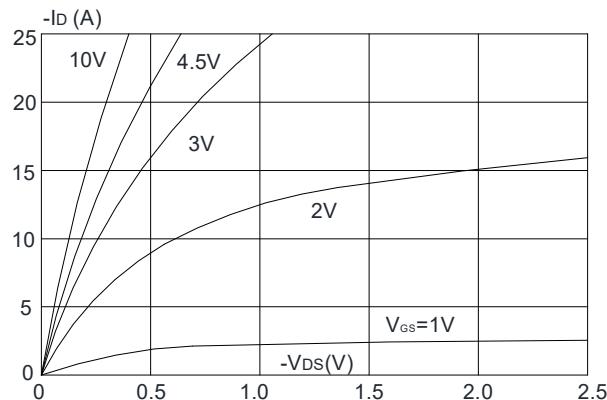


Figure 3: On-resistance vs. Drain Current

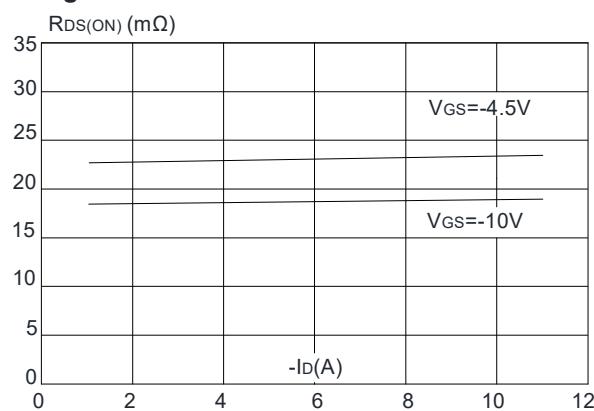


Figure 5: Gate Charge Characteristics

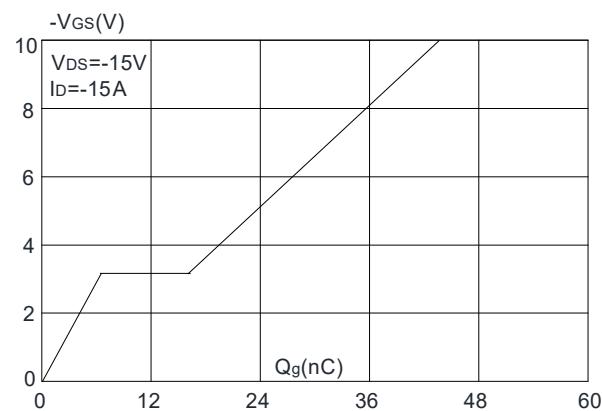


Figure 2: Typical Transfer Characteristics

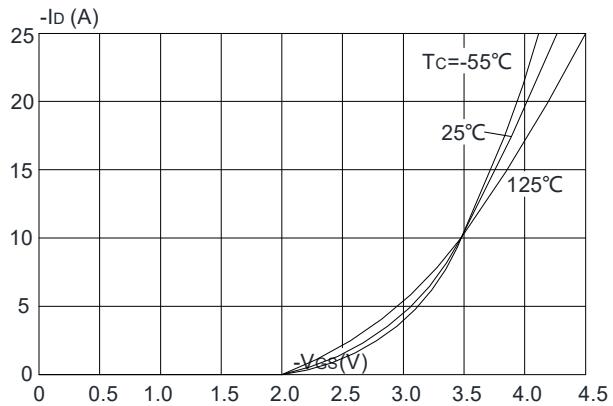


Figure 4: Body Diode Characteristics

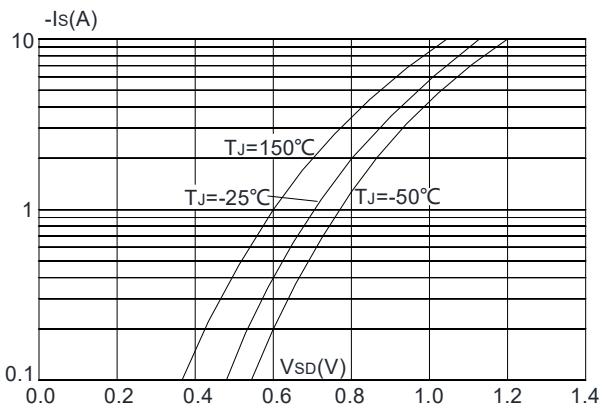


Figure 6: Capacitance Characteristics

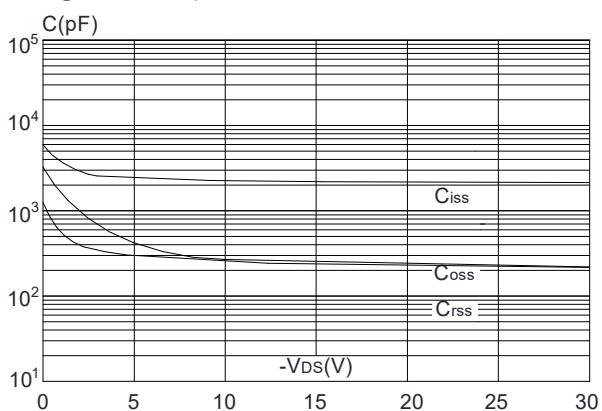


Figure 7: Normalized Breakdown Voltage vs. Junction Temperature

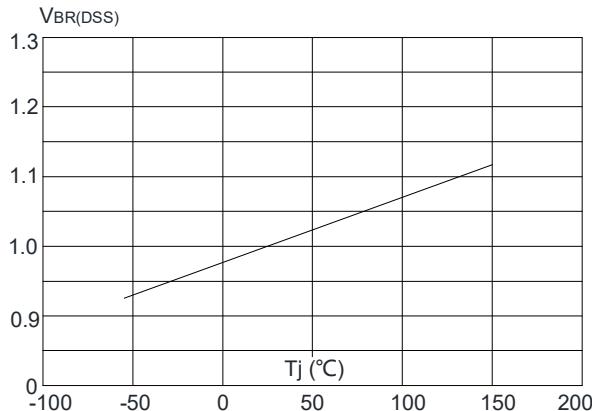


Figure 8: Normalized on Resistance vs. Junction Temperature

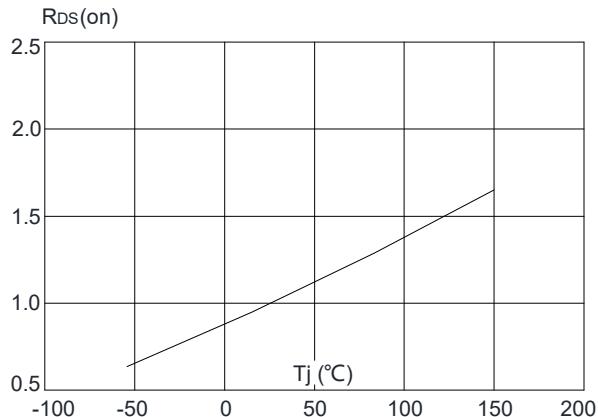


Figure 9: Maximum Safe Operating Area

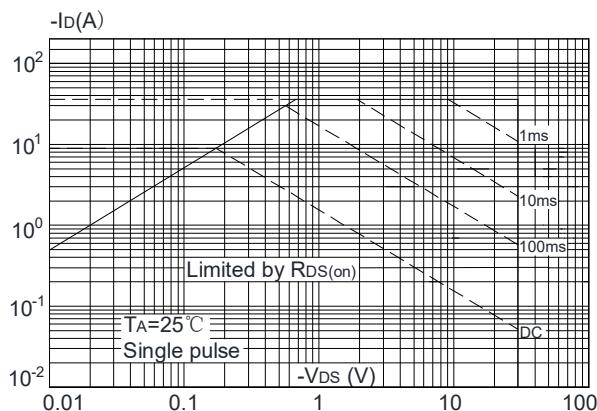


Figure 10: Maximum Continuous Drain Current vs. Ambient Temperature

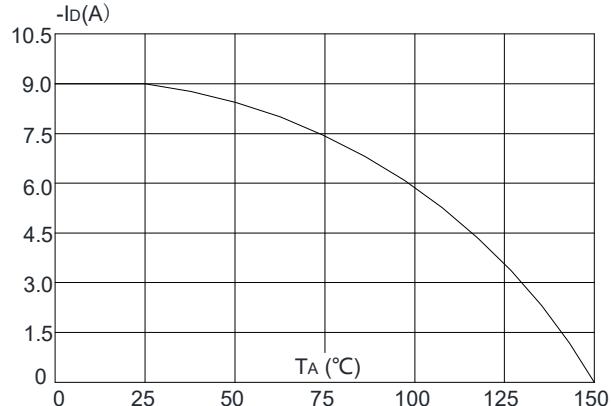
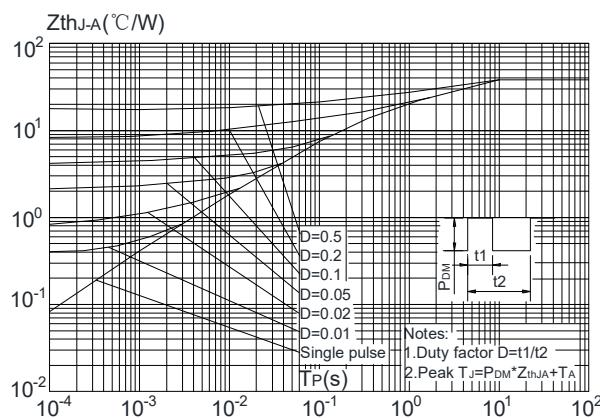
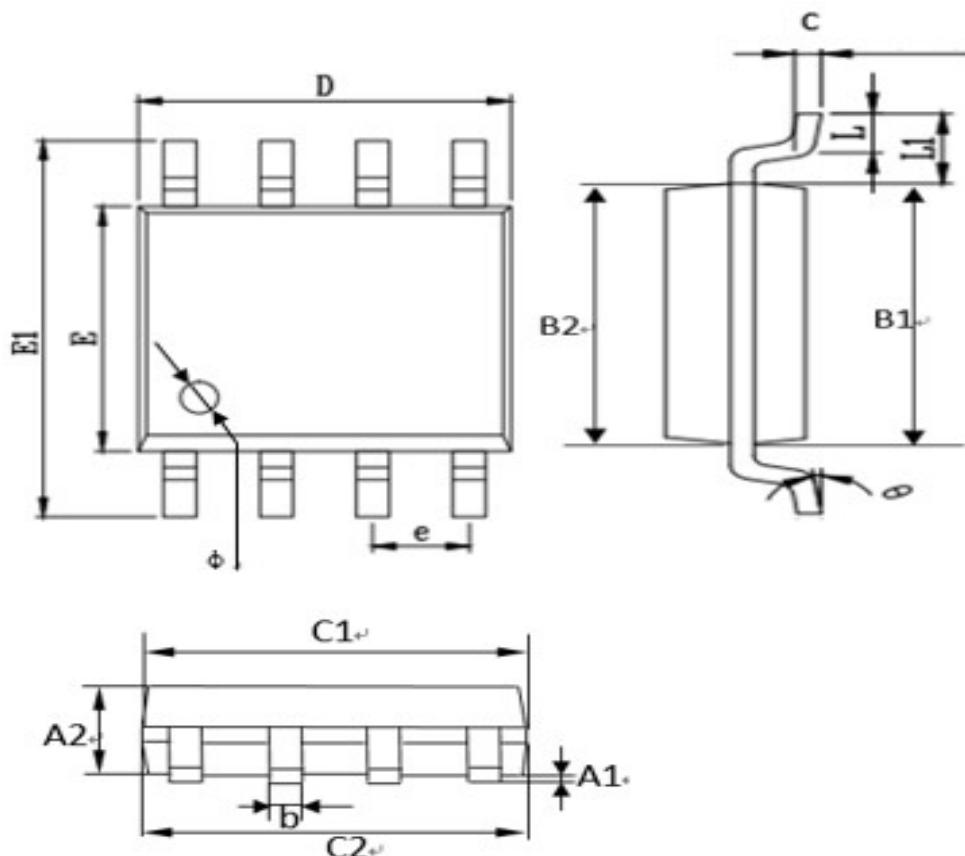


Figure 11: Maximum Effective Transient Thermal Impedance, Junction-to-Ambient



SOP-8 Package Information



符号	标准	下公差	上公差	下限值	上限值
A1	0.11	0.07	0.07	0.04	0.18
A2	1.4	0.1	0.1	1.3	1.5
B1	3.9	0.1	0.1	3.8	4.0
B2	3.85	0.1	0.1	3.75	3.95
b	0.42	0.05	0.05	0.37	0.47
C1	4.85	0.2	0.2	4.65	5.05
C2	4.9	0.2	0.2	4.7	5.1
c	0.21	0.03	0.03	0.18	0.24
D	4.9	0.2	0.2	4.7	5.1
E	3.9	0.2	0.2	3.7	4.1
E1	6.0	0.2	0.2	5.8	6.2
e	1.27	0.03	0.03	1.24	1.30
L	0.5	0.1	0.1	0.4	0.6
*L1	1.05	0.06	0.06	0.99	1.11
θ_1	4°	4°	4°	0°	8°

Revision History

Revision	Release	Remark
V1.0	2023/04/03	Initial Release

Disclaimer

The information given in this document describes the independent performance of the product, but similar performance is not guaranteed under other working conditions, and cannot be guaranteed when installed with other products or equipment. To achieve the required performance of the product in actual scenarios, the customer should conduct a complete application test to assess the functionality of the product.

Allpower assumes no responsibility for equipment failures result from using products at values that exceed the ratings, operating conditions, or other parameters listed in the product specifications.

The product described in this specification is not applicable for aerospace or other applications which requires high reliability. Customers using or selling these products for use in medical, life-saving, or life-sustaining applications do so at their own risk and agree to fully indemnify.

Due to product or technical improvements, the information described or contained herein may be changed without prior notice.