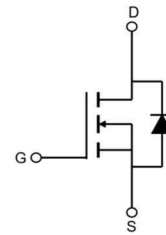


Feature

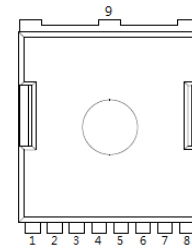
- 100V,210A
 $R_{DS(ON)} < 2.8m\Omega @ V_{GS}=10V$ (TYP:2.2m Ω)
- Split Gate Trench Technology
- Lead free product is acquired
- Excellent $R_{DS(ON)}$ and Low Gate Charge



Schematic Diagram

Application

- PWM applications
- Load Switch
- Power management



TOLL-8L

1	Gate(G)
2,3,4,5,6,7,8	Source(S)
9	Drain(D)

Package Marking and Ordering Information

Device Marking	Device	Device Package	Reel Size	Tape width	Quantity (PCS)
G028N10T	APG028N10T	TOLL-8L	-	-	2000

ABSOLUTE MAXIMUM RATINGS (T_J=25°C unless otherwise noted)

Parameter	Symbol	Value	Unit
Drain-Source Voltage	V _{DS}	100	V
Gate-Source Voltage	V _{GS}	±20	V
Continuous Drain Current (Tc =25°C)	I _D	210	A
Continuous Drain Current (Tc =100°C)	I _D	132	A
Pulsed Drain Current ⁽¹⁾	I _{DM}	840	A
Single Pulsed Avalanche Energy ⁽²⁾	E _{AS}	418	mJ
Power Dissipation	P _D	272	W
Thermal Resistance from Junction to Case	R _{θJC}	0.46	°C/W
Thermal Resistance from Junction to Ambient	R _{θJA}	50	°C/W
Junction Temperature	T _J	150	°C
Storage Temperature	T _{STG}	-55~ +150	°C

MOSFET ELECTRICAL CHARACTERISTICS(T_J=25°C unless otherwise noted)

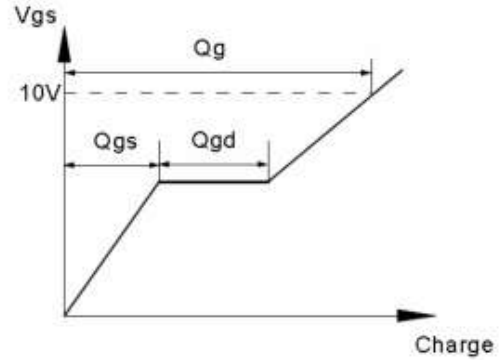
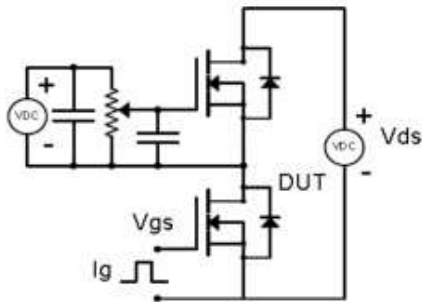
Parameter	Symbol	Test Condition	Min	Type	Max	Unit
Static Characteristics						
Drain-source breakdown voltage	V _{(BR)DSS}	V _{GS} = 0V, I _D =250μA	100	-	-	V
Zero gate voltage drain current	I _{DSS}	V _{DS} =100V, V _{GS} = 0V	-	-	1	μA
Gate-body leakage current	I _{GSS}	V _{GS} =±20V, V _{DS} = 0V	-	-	±100	nA
Gate threshold voltage ⁽³⁾	V _{GS(th)}	V _{DS} =V _{GS} , I _D =250μA	2	3	4	V
Drain-source on-resistance ⁽³⁾	R _{DS(on)}	V _{GS} =10V, I _D =20A	-	2.2	2.8	mΩ
Gate Resistance	R _g	V _{DS} =V _{GS} =0V, f =1MHz	-	2.7	-	Ω
Dynamic characteristics						
Input Capacitance	C _{iss}	V _{DS} =50V, V _{GS} =0V, f =1MHz	-	8390	-	pF
Output Capacitance	C _{oss}		-	2780	-	
Reverse Transfer Capacitance	C _{rss}		-	127	-	
Switching characteristics						
Turn-on delay time	t _{d(on)}	V _{DD} =50V, I _D =50A, V _{GS} =10V, R _G =3Ω	-	33	-	ns
Turn-on rise time	t _r		-	28	-	
Turn-off delay time	t _{d(off)}		-	102	-	
Turn-off fall time	t _f		-	36	-	
Total Gate Charge	Q _g	V _{DS} =50V, I _D =50A, V _{GS} =10V	-	112	-	nC
Gate-Source Charge	Q _{gs}		-	31	-	
Gate-Drain Charge	Q _{gd}		-	26	-	
Reverse Recovery Chrage	Q _{rr}	I _F =20A, di/dt=100A/us		178		nC
Reverse Recovery Time	T _{rr}	I _F =20A, di/dt=100A/us		89		ns
Source-Drain Diode characteristics						
Diode Forward voltage ⁽³⁾	V _{DS}	V _{GS} =0V, I _S =40A	-	0.8	1.2	V
Diode Forward current ⁽⁴⁾	I _S		-	-	210	A

Notes:

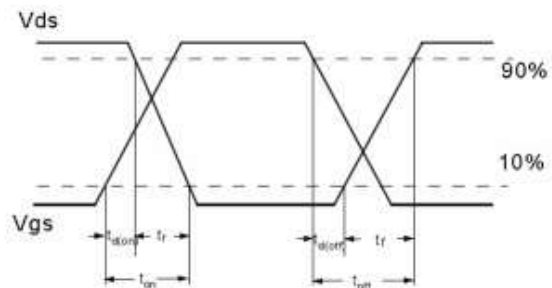
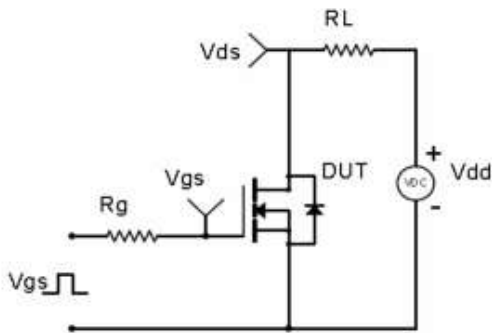
1. Repetitive Rating: pulse width limited by maximum junction temperature
2. EAS Condition: T_J=25°C, V_{DD}=50V, R_G=25 Ω, L=0.5Mh
3. Pulse Test: pulse width≤300μs, duty cycle≤2%
4. Surface Mounted on FR4 Board, t≤10 sec

Test Circuit & Waveform

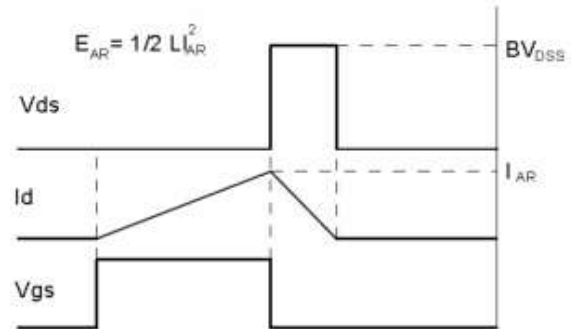
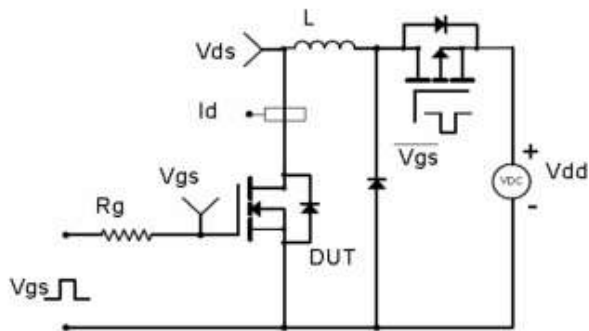
Gate Charge Test Circuit & Waveform



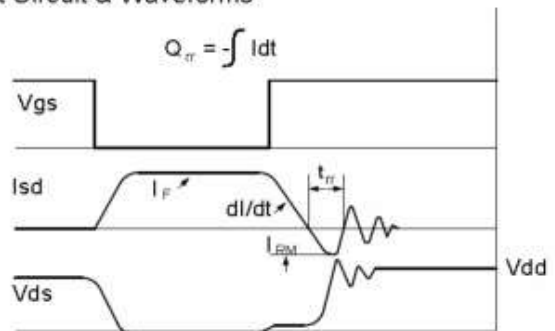
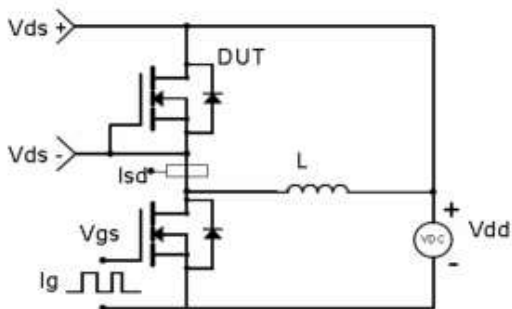
Resistive Switching Test Circuit & Waveforms



Unclamped Inductive Switching (UIS) Test Circuit & Waveforms



Diode Recovery Test Circuit & Waveforms



Typical Performance Characteristics

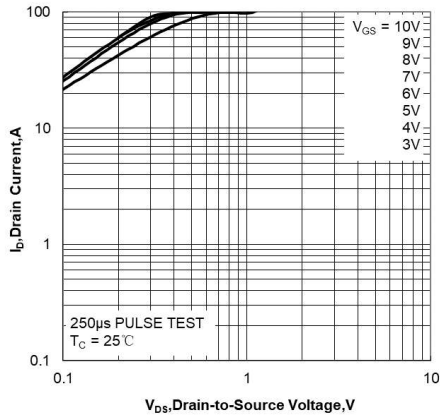


Figure 1. Output Characteristics

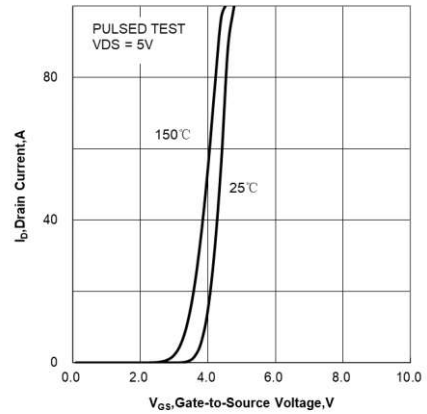


Figure 2. Transfer Characteristics

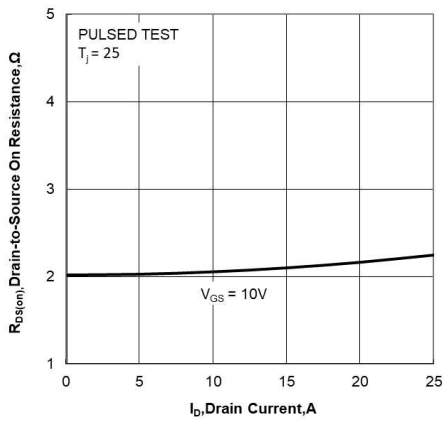


Figure 3. Drain-to-Source On Resistance vs Drain Current

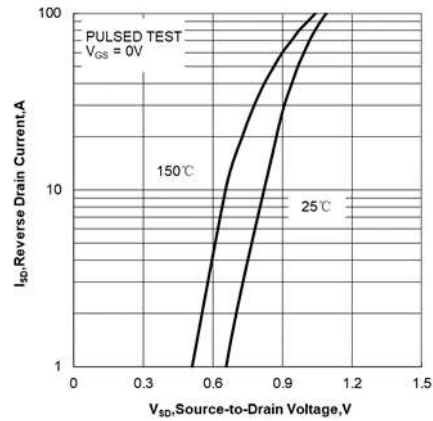


Figure 4. Body Diode Forward Voltage vs Source Current and Temperature

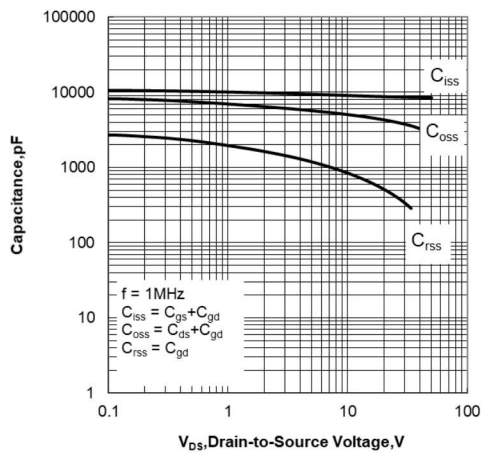


Figure 5. Capacitance Characteristics

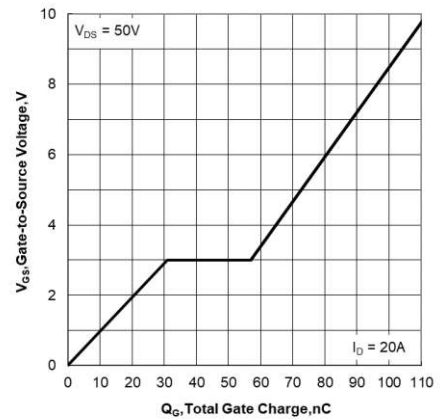


Figure 6. Gate Charge Characteristics

Typical Performance Characteristics

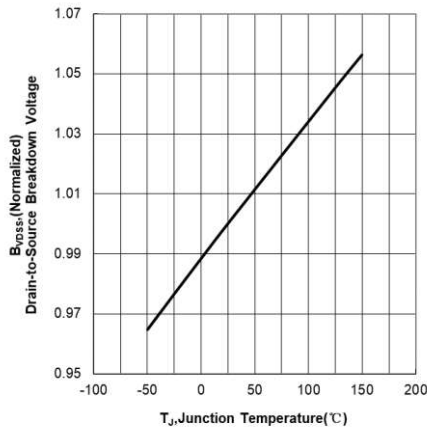


Figure 7. Normalized Breakdown Voltage vs Junction Temperature

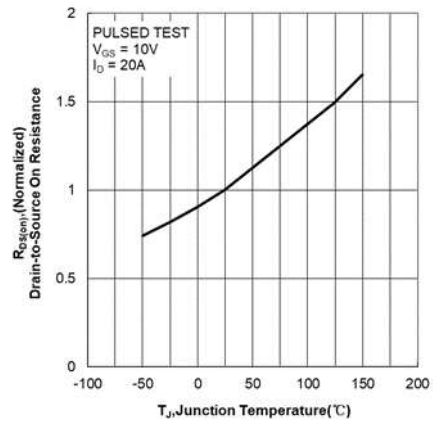


Figure 8. Normalized On Resistance vs Junction Temperature

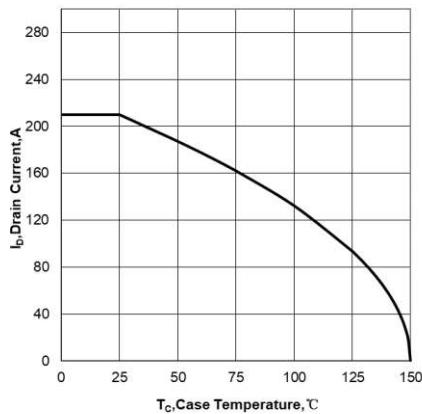


Figure 9. Maximum Continuous Drain Current vs Case Temperature

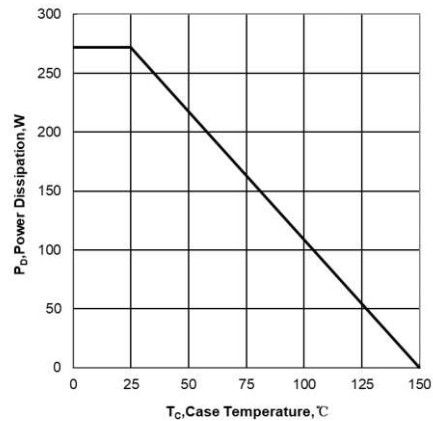


Figure 10. Maximum Power Dissipation vs Case Temperature

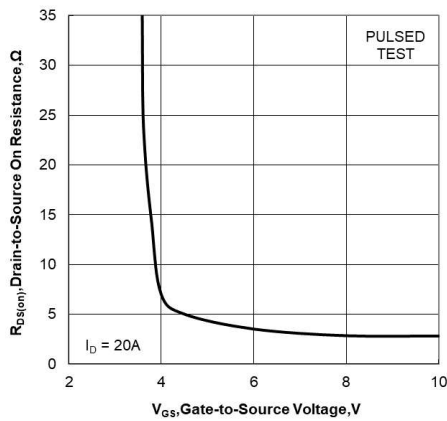


Figure 11. Drain-to-Source On Resistance vs Gate Voltage and Drain Current

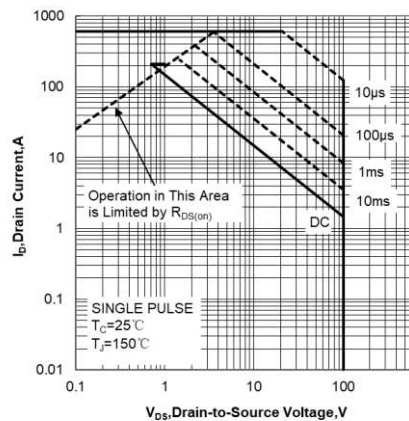


Figure 12. Maximum Safe Operating Area

Typical Performance Characteristics

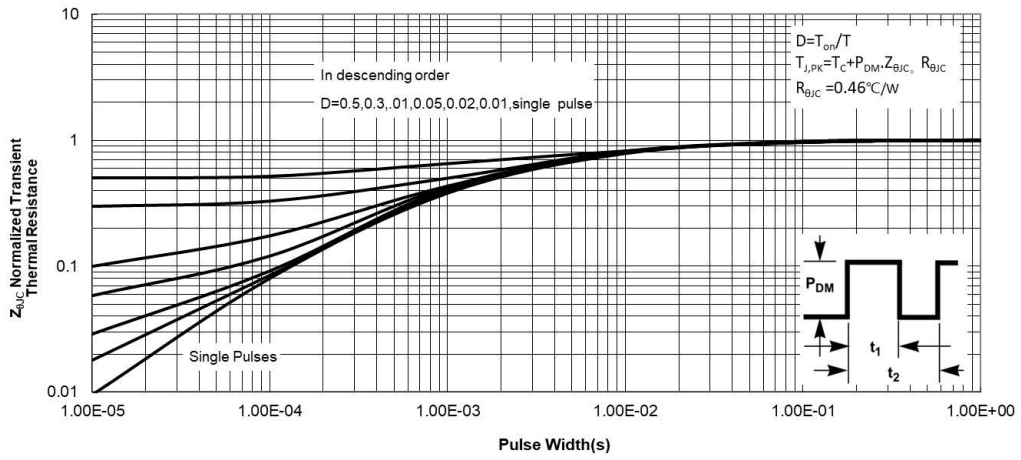
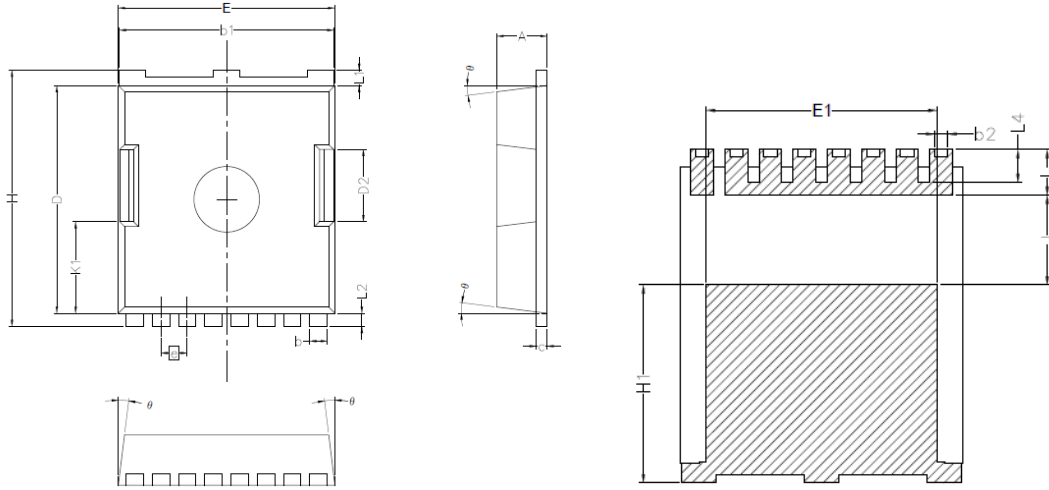


Figure 13. Maximum Effective Transient Thermal Impedance, Junction-to-Case

Package Dimensions

TOLL-8L



Symbol	Dimensions In Millimeters	
	MIN.	MAX.
A	2.20	2.40
b	0.90	0.90
b1	9.70	9.90
b2	0.42	0.50
c	0.40	0.60
D	10.28	10.58
D2	3.10	3.50
E	9.70	10.10
E1	7.90	8.30
e	1.20BSC	
H	11.48	11.88
H1	6.75	7.15
N	8	
J	3.00	3.30
K1	3.98	4.38
L	1.40	1.80
L1	0.60	0.80
L2	0.50	0.70
L4	1.00	1.30
θ	4°	10°