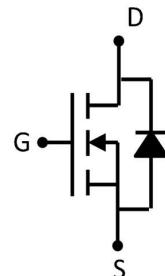
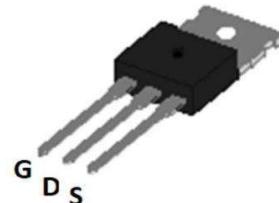


## Feature

- 100V,65A
- $R_{DS(ON)} < 9.5\text{ m}\Omega$  @  $V_{GS}=10\text{ V}$  (TYP:8.0m $\Omega$ )
- $R_{DS(ON)} < 13\text{ m}\Omega$  @  $V_{GS}=4.5\text{ V}$  (TYP:11m $\Omega$ )
- Split Gate Trench Technology
- Lead free product is acquired
- Excellent  $R_{DS(ON)}$  and Low Gate Charge



Schematic Diagram



TO-220

## Application

- PWM applications
- Load Switch
- Power management

## Package Marking and Ordering Information

Device Marking	Device	Device Package	Reel Size	Tape width	Quantity (PCS)
G095N01	APG095N01	TO-220		-	1000

## ABSOLUTE MAXIMUM RATINGS ( $T_a=25^\circ\text{C}$ unless otherwise noted)

Parameter	Symbol	Value	Unit
Drain-Source Voltage	$V_{DS}$	100	V
Gate-Source Voltage	$V_{GS}$	$\pm 20$	V
Continuous Drain Current ( $T_a = 25^\circ\text{C}$ )	$I_D$	65	A
Continuous Drain Current ( $T_a = 100^\circ\text{C}$ )	$I_D$	46	A
Pulsed Drain Current <sup>(1)</sup>	$I_{DM}$	200	A
Single Pulsed Avalanche Energy <sup>(2)</sup>	$E_{AS}$	90	mJ
Power Dissipation	$P_D$	120	W
Thermal Resistance from Junction to Ambient	$R_{\theta JA}$	62.5	$^\circ\text{C}/\text{W}$
Junction Temperature	$T_J$	150	$^\circ\text{C}$
Storage Temperature	$T_{STG}$	-55~+150	$^\circ\text{C}$

**MOSFET ELECTRICAL CHARACTERISTICS( $T_a=25^\circ C$  unless otherwise noted)**

Parameter	Symbol	Test Condition	Min	Type	Max	Unit
<b>Static Characteristics</b>						
Drain-source breakdown voltage	$V_{(BR)DSS}$	$V_{GS} = 0V, I_D = 250\mu A$	100	-	-	V
Zero gate voltage drain current	$I_{DSS}$	$V_{DS} = 80V, V_{GS} = 0V$	-	-	1	$\mu A$
Gate-body leakage current	$I_{GSS}$	$V_{GS} = \pm 20V, V_{DS} = 0V$	-	-	$\pm 100$	nA
Gate threshold voltage <sup>(3)</sup>	$V_{GS(th)}$	$V_{DS} = V_{GS}, I_D = 250\mu A$	1.2	1.8	2.5	V
Drain-source on-resistance <sup>(3)</sup>	$R_{DS(on)}$	$V_{GS} = 10V, I_D = 20A$	-	8.0	9.5	$m\Omega$
		$V_{GS} = 4.5V, I_D = 10A$	-	11	13	
Forward Threshold Voltage	$g_{fs}$	$V_{DS} = 5V, I_D = 20A$	-	13.5	-	S
Gate Resistance	$R_g$	$V_{DS} = V_{GS} = 0V, f = 1MHz$	-	1.94	-	$\Omega$
<b>Dynamic characteristics</b>						
Input Capacitance	$C_{iss}$	$V_{DS} = 50V, V_{GS} = 0V, f = 1MHz$	-	2022	-	$pF$
Output Capacitance	$C_{oss}$		-	580	-	
Reverse Transfer Capacitance	$C_{rss}$		-	28	-	
<b>Switching characteristics</b>						
Turn-on delay time	$t_{d(on)}$	$V_{DD} = 50V, I_D = 20A,$ $V_{GS} = 10V, R_G = 3\Omega$	-	17	-	$ns$
Turn-on rise time	$t_r$		-	4	-	
Turn-off delay time	$t_{d(off)}$		-	32	-	
Turn-off fall time	$t_f$		-	8	-	
Total Gate Charge	$Q_g$	$V_{DS} = 50V, I_D = 20A,$ $V_{GS} = 10V$	-	38.5	-	$nC$
Gate-Source Charge	$Q_{gs}$		-	8	-	
Gate-Drain Charge	$Q_{gd}$		-	9	-	
Reverse Recovery Charge	$Q_{rr}$	$I_F = 20A, di/dt = 100A/us$		68		$nC$
Reverse Recovery Time	$T_{rr}$	$I_F = 20A, di/dt = 100A/us$		50.5		$ns$
<b>Source-Drain Diode characteristics</b>						
Diode Forward voltage <sup>(3)</sup>	$V_{DS}$	$V_{GS} = 0V, I_S = 20A$	-	-	1.2	V
Diode Forward current <sup>(4)</sup>	$I_S$		-	-	60	A

**Notes:**

1. Repetitive Rating: pulse width limited by maximum junction temperature
2. EAS Condition:  $T_J = 25^\circ C, V_{DD} = 50V, R_G = 25\Omega, L = 0.5mH$
3. Pulse Test: pulse width  $\leq 300\mu s$ , duty cycle  $\leq 2\%$
4. Surface Mounted on FR4 Board,  $t \leq 10$  sec

## Typical Performance Characteristics

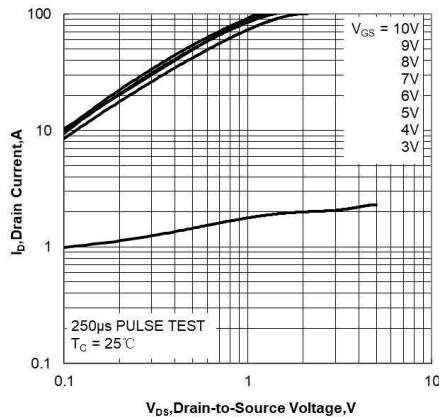


Figure 1. Output Characteristics

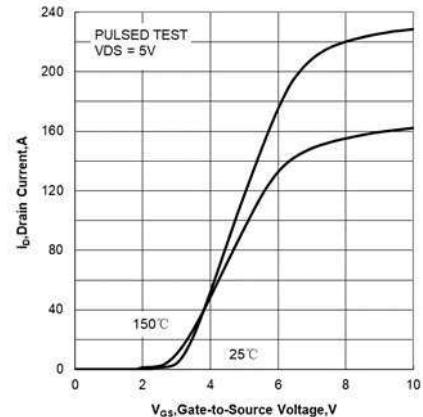


Figure 2. Transfer Characteristics

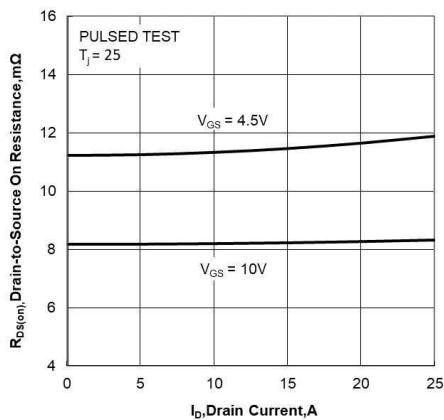
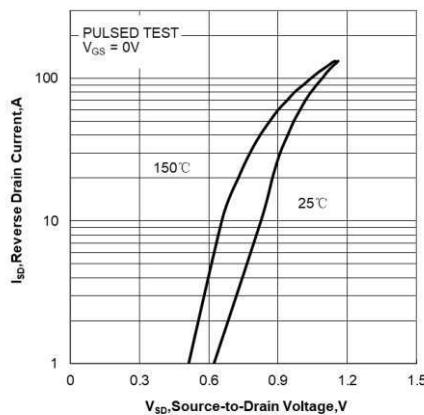
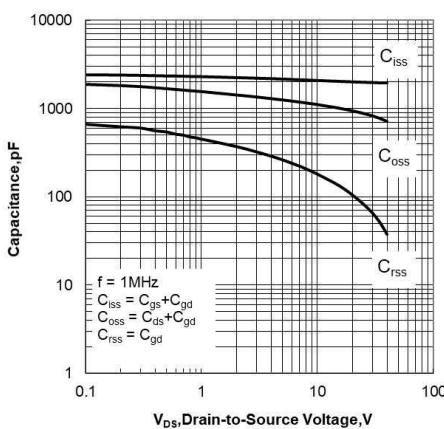
Figure 3. Drain-to-Source On Resistance  
vs Drain CurrentFigure 4. Body Diode Forward Voltage  
vs Source Current and Temperature

Figure 5. Capacitance Characteristics

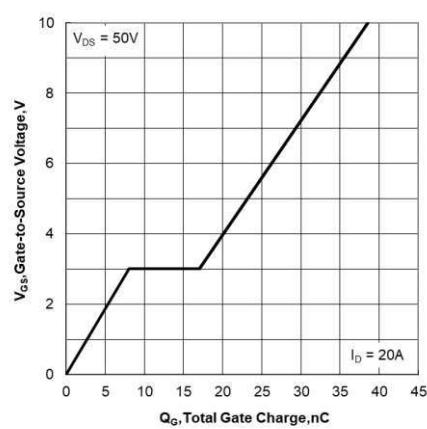
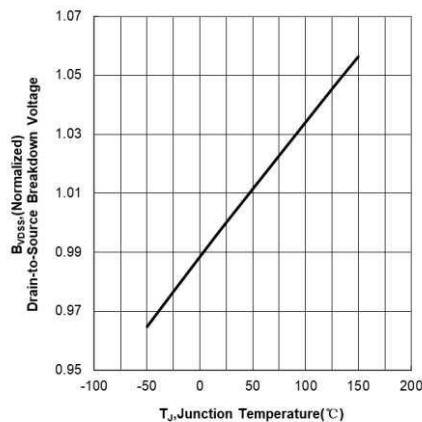
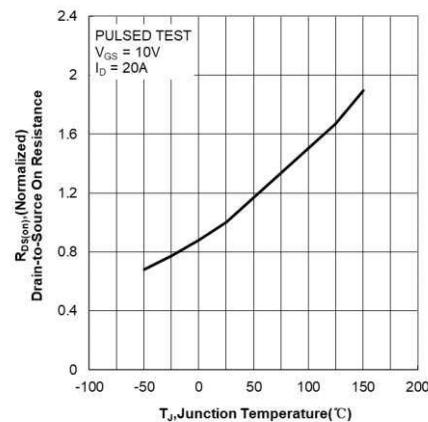


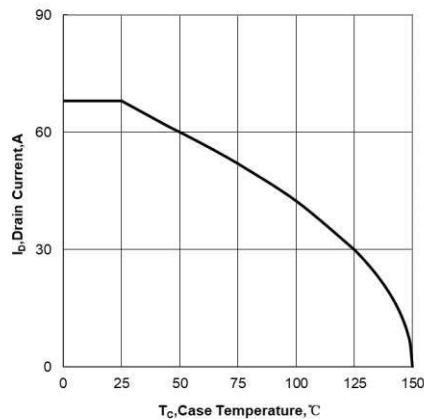
Figure 6. Gate Charge Characteristics



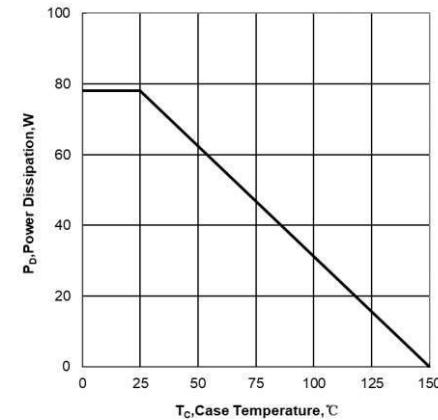
**Figure 7. Normalized Breakdown Voltage  
vs Junction Temperature**



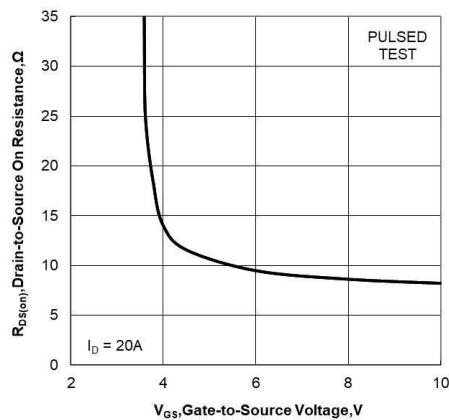
**Figure 8. Normalized On Resistance vs  
Junction Temperature**



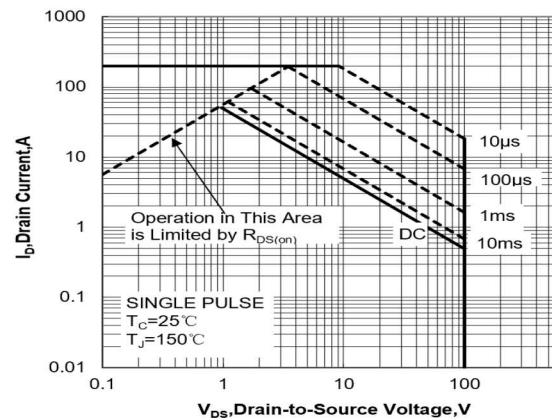
**Figure 9. Maximum Continuous Drain Current  
vs Case Temperature**



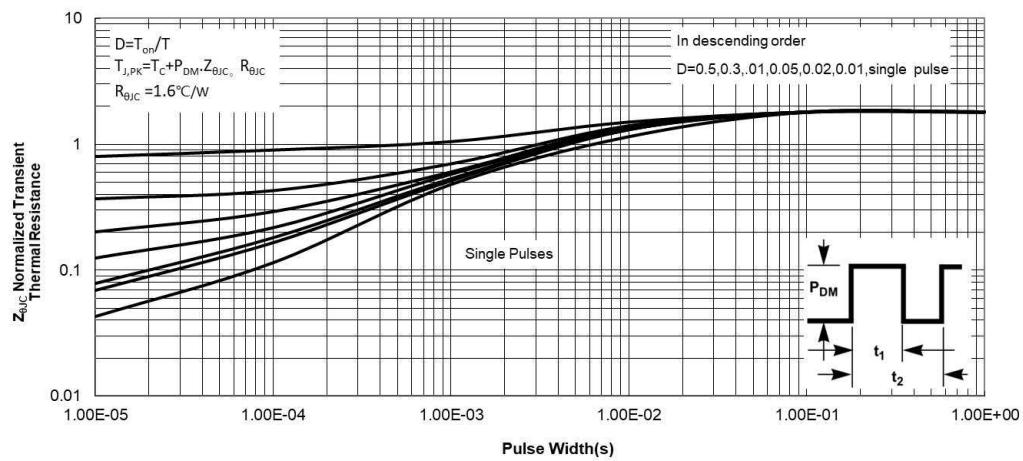
**Figure 10. Maximum Power Dissipation  
vs Case Temperature**



**Figure 11. Drain-to-Source On Resistance vs Gate  
Voltage and Drain Current**

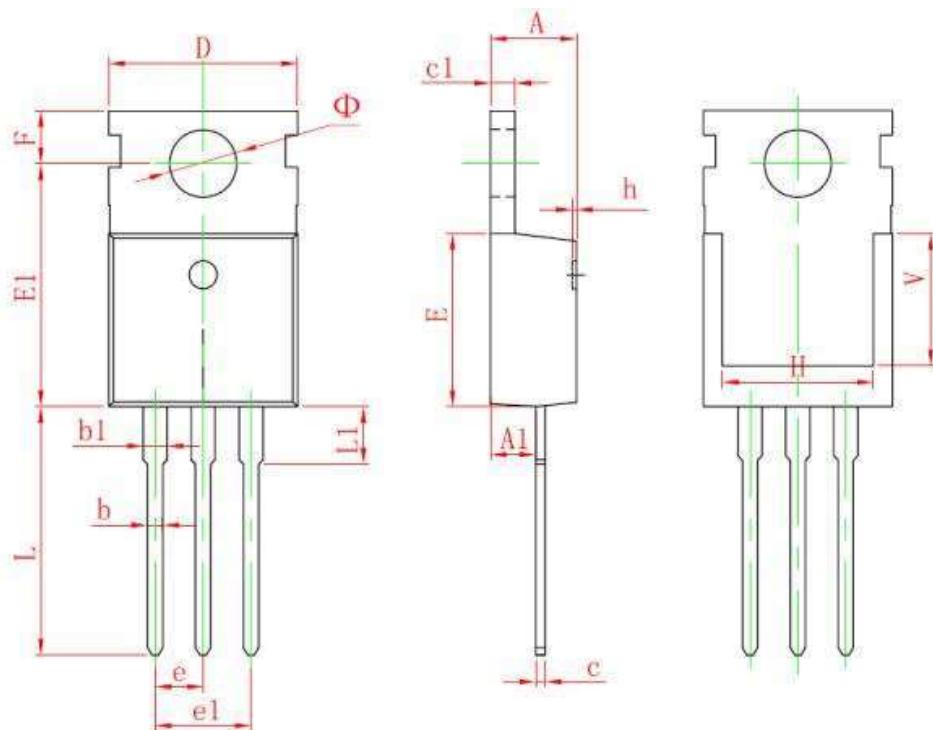


**Figure 12. Maximum Safe Operating Area**



**Figure 13. Maximum Effective Transient Thermal Impedance, Junction-to-Case**

## TO220 Package Information



<b>Symbol</b>	<b>Dimensions In Millimeters</b>		<b>Dimensions In Inches</b>	
	<b>Min.</b>	<b>Max.</b>	<b>Min.</b>	<b>Max.</b>
A	4.400	4.600	0.173	0.181
A1	2.250	2.550	0.089	0.100
b	0.710	0.910	0.028	0.036
b1	1.170	1.370	0.046	0.054
c	0.330	0.650	0.013	0.026
c1	1.200	1.400	0.047	0.055
D	9.910	10.250	0.390	0.404
E	8.950	9.750	0.352	0.384
E1	12.650	13.050	0.498	0.514
e	2.540 TYP.		0.100 TYP.	
e1	4.980	5.180	0.196	0.204
F	2.650	2.950	0.104	0.116
H	7.900	8.100	0.311	0.319
h	0.000	0.300	0.000	0.012
L	12.900	13.400	0.508	0.528
L1	2.850	3.250	0.112	0.128
V	6.900 REF.		0.276 REF.	
Φ	3.400	3.800	0.134	0.150