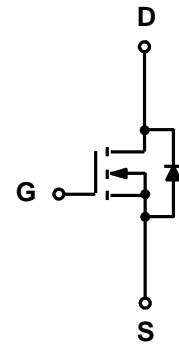


Features

- 100V,220A
 $R_{DS(on)} < 2.8m\Omega$ @ $V_{GS}=10V$ TYP: $2.1m\Omega$
- Split Gate Trench Technology
- Fast Switching
- Low On-Resistance
- Low Gate Charge
- Low Reverse transfer capacitances
- High avalanche ruggedness



TO-247

Applications

- DC/DC Converter
- LED Backlighting
- Power Management Switches

Package Marking and Ordering Information

Device Marking	Device	Device Package	Reel Size	Tape width	Quantity (PCS)
G028N10W	APG028N10W	TO-247	-	-	600

ABSOLUTE MAXIMUM RATINGS ($T_J=25^\circ C$ unless otherwise noted)

Parameter	Symbol	Value	Unit
Drain-Source Voltage	V_{DS}	100	V
Gate-Source Voltage	V_{GS}	± 20	V
Continuous Drain Current ($T_c=25^\circ C$) ⁽¹⁾	I_D	220	A
Continuous Drain Current ($T_c=100^\circ C$)	I_D	180	A
Pulsed Drain Current	I_{DM}	880	A
Drain Power Dissipation ⁽⁴⁾	P_D	296	W
Single Pulsed Avalanche Energy	E_{AS}	500	mJ
Thermal Resistance from Junction to Case ⁽¹⁾	$R_{\theta JC}$	0.42	$^\circ C/W$
Thermal Resistance from Junction to Ambient	$R_{\theta JA}$	40	$^\circ C/W$
Junction Temperature	T_J	-55~+150	$^\circ C$
Storage Temperature	T_{STG}	-55~+150	$^\circ C$

MOSFET ELECTRICAL CHARACTERISTICS($T_J=25^\circ\text{C}$ unless otherwise noted)

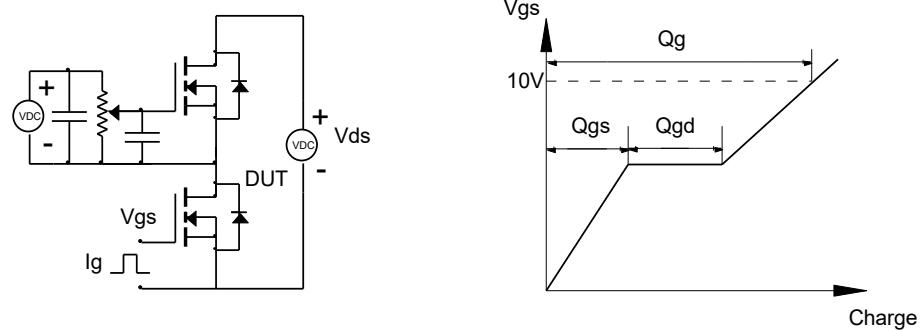
Parameter	Symbol	Test Condition	Min	Type	Max	Unit
Static Characteristics						
Drain-source breakdown voltage	$V_{(\text{BR})\text{DSS}}$	$V_{\text{GS}} = 0\text{V}, I_D = 250\mu\text{A}$	100	-	-	V
Zero gate voltage drain current	I_{DSS}	$V_{\text{DS}} = 100\text{V}, V_{\text{GS}} = 0\text{V}$	-	-	1	μA
Gate-body leakage current	I_{GSS}	$V_{\text{GS}} = \pm 20\text{V}, V_{\text{DS}} = 0\text{V}$	-	-	± 100	nA
Gate threshold voltage	$V_{\text{GS}(\text{th})}$	$V_{\text{DS}} = V_{\text{GS}}, I_D = 250\mu\text{A}$	2	3	4	V
Drain-source on-resistance ⁽²⁾	$R_{\text{DS}(\text{on})}$	$V_{\text{GS}} = 10\text{V}, I_D = 20\text{A}$	-	2.1	2.8	$\text{m}\Omega$
Dynamic characteristics						
Input Capacitance	C_{iss}	$V_{\text{DS}} = 50\text{V}, V_{\text{GS}} = 0\text{V}, f = 1\text{MHz}$	-	8800	-	pF
Output Capacitance	C_{oss}		-	1290	-	
Reverse Transfer Capacitance	C_{rss}		-	40	-	
Switching characteristics						
Turn-on delay time	$t_{\text{d}(\text{on})}$	$V_{\text{DD}} = 50\text{V}, I_D = 20\text{A}, R_G = 3\Omega, V_{\text{GS}} = 10\text{V}$	-	30.8	-	nS
Turn-on rise time	t_r		-	26	-	
Turn-off delay time	$t_{\text{d}(\text{off})}$		-	68	-	
Turn-off fall time	t_f		-	12.4	-	
Total Gate Charge	Q_g	$V_{\text{DS}} = 50\text{V}, I_D = 20\text{A}, V_{\text{GS}} = 10\text{V}$	-	150	-	nC
Gate-Source Charge	Q_{gs}		-	34	-	
Gate-Drain Charge	Q_{gd}		-	26	-	
Source-Drain Diode characteristics						
Diode Forward voltage ⁽²⁾	V_{SD}	$T_J = 25^\circ\text{C}, V_{\text{GS}} = 0\text{V}, I_s = 20\text{A}$	-	-	1.2	V
Diode Forward current	I_s	$T_c = 25^\circ\text{C}$	-	-	220	A
Body Diode Reverse Recovery Time	trr	$T_J = 25^\circ\text{C}, I_F = 20\text{A}, dI/dt = 100\text{A}/\mu\text{s}$	-	110	-	nS
Body Diode Reverse Recovery Charge	Qrr		-	202	-	nC

Notes:

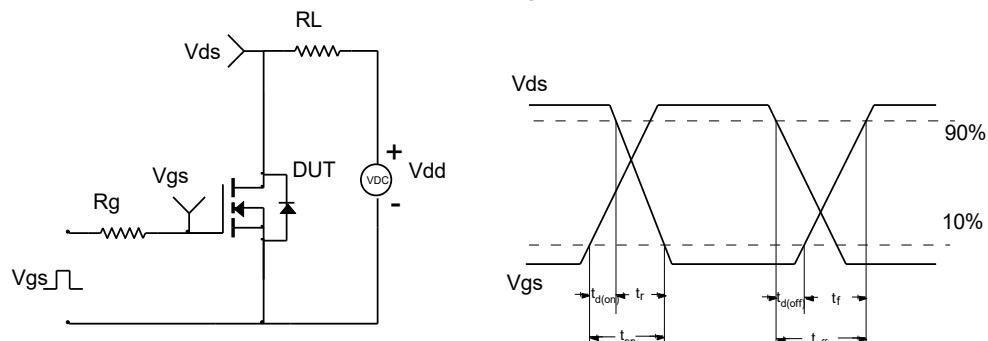
1. The data tested by surface mounted on a 1 inch² FR-4 board with 2OZ copper.
2. The data tested by pulsed , pulse width $\leq 300\mu\text{s}$, duty cycle $\leq 2\%$
3. The EAS data shows Max. rating. The test condition is $V_{\text{DD}}=50\text{V}, V_{\text{GS}}=10\text{V}, L=0.4\text{mH}, I_{\text{AS}}=64\text{A}$
4. The power dissipation is limited by 150°C junction temperature
5. The data is theoretically the same as ID and IDM , in real applications , should be limited by total power dissipation.

Test Circuit

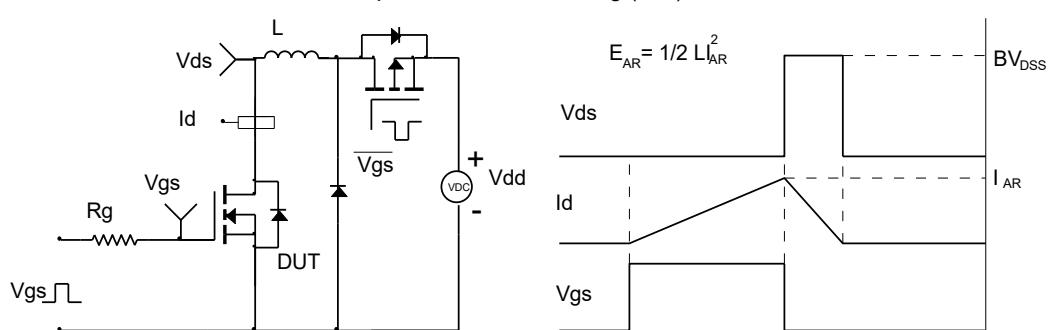
Gate Charge Test Circuit & Waveform



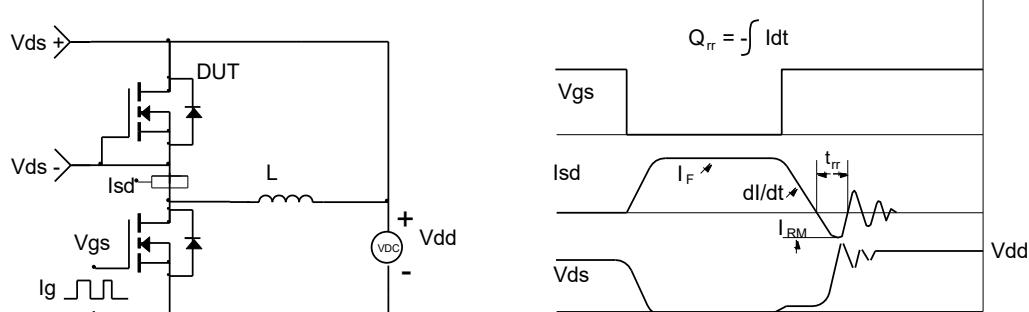
Resistive Switching Test Circuit & Waveforms



Unclamped Inductive Switching (UIS) Test Circuit & Waveforms



Diode Recovery Test Circuit & Waveforms



Typical Characteristics

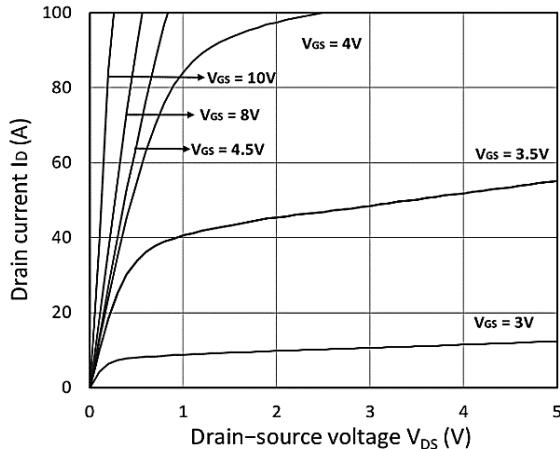


Figure 1. Output Characteristics

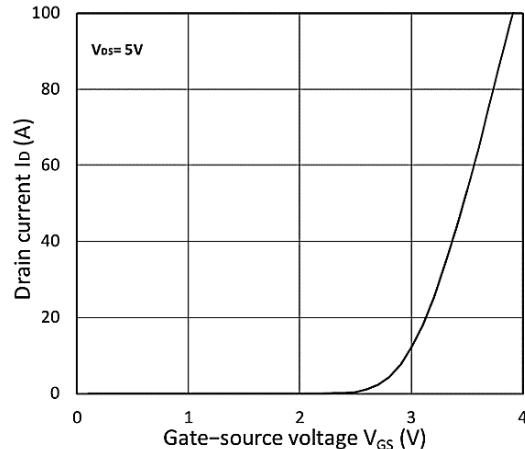


Figure 2. Transfer Characteristics

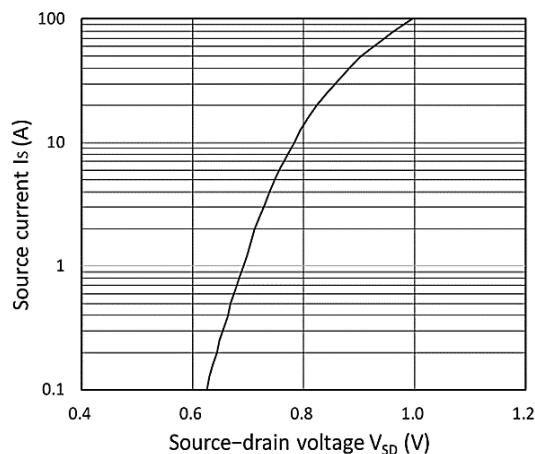


Figure 3. Forward Characteristics of Reverse

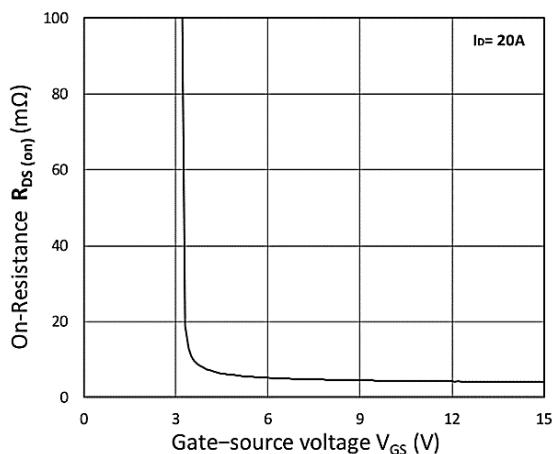


Figure 4. $R_{DS(ON)}$ vs. V_{GS}

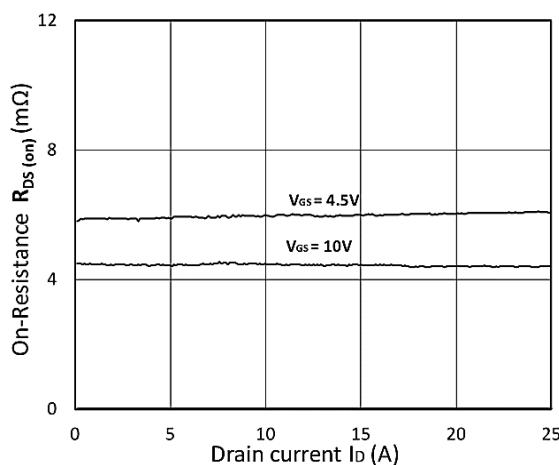


Figure 5. $R_{DS(ON)}$ vs. I_D

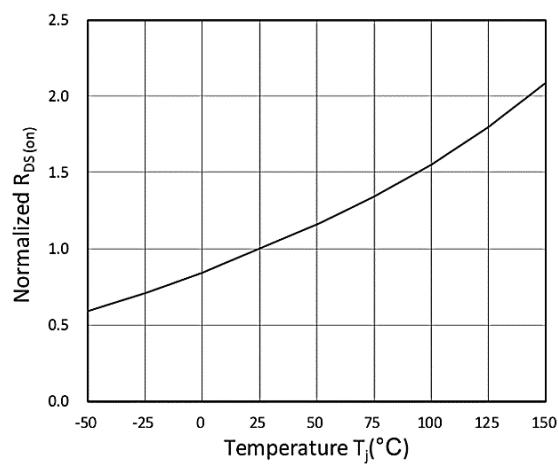


Figure 6. Normalized $R_{DS(ON)}$ vs. Temperature

Typical Characteristics

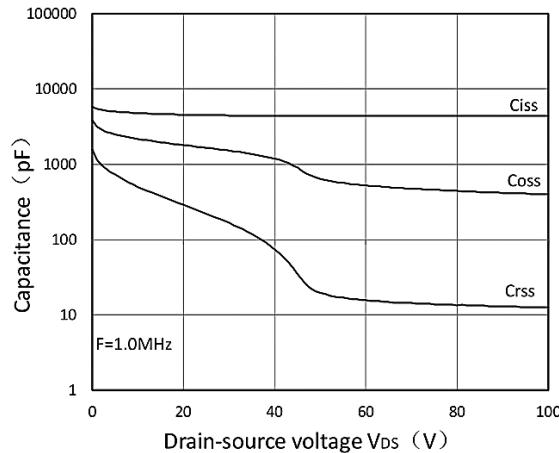


Figure 7. Capacitance Characteristics

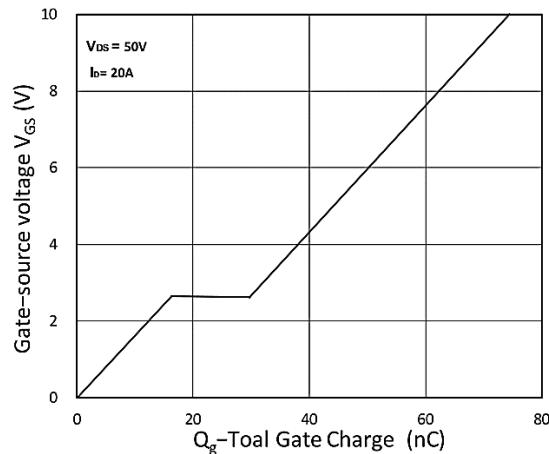


Figure 8. Gate Charge Characteristics

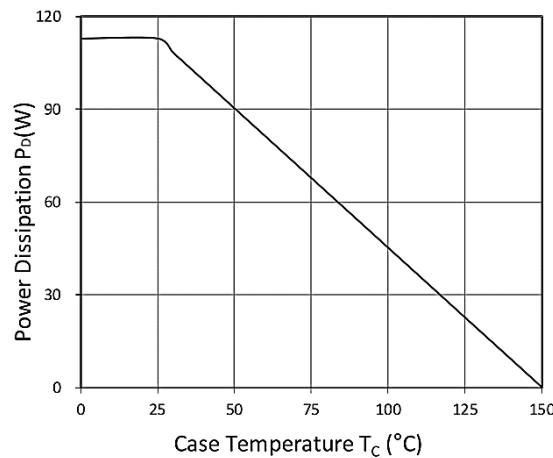


Figure 9. Power Dissipation

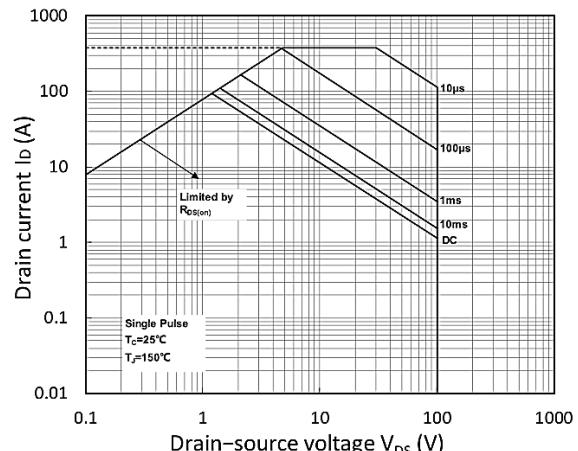


Figure10. Safe Operating Area

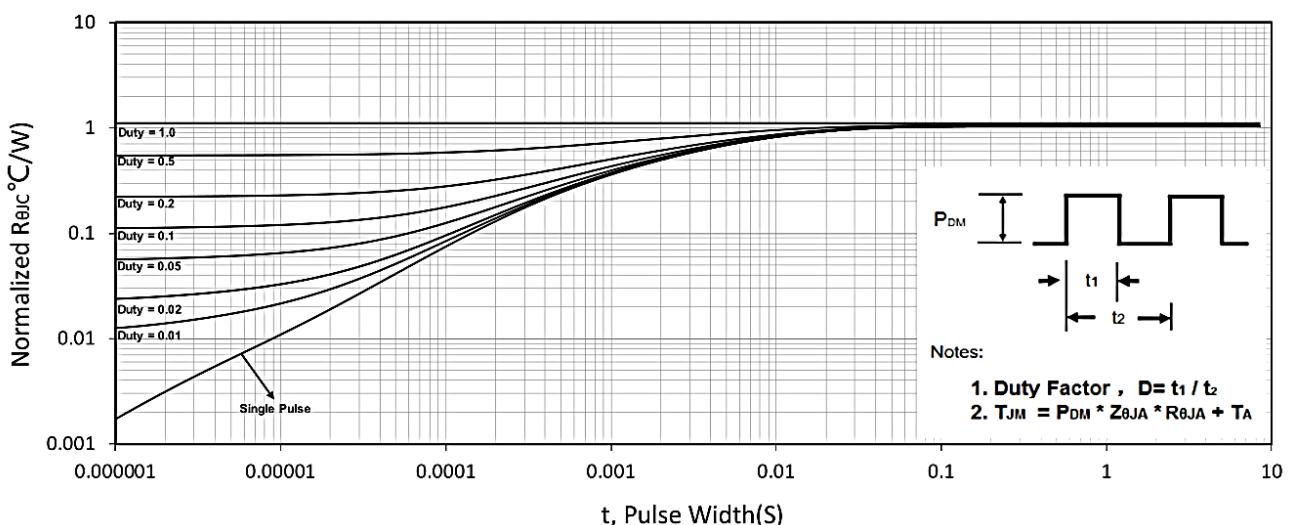
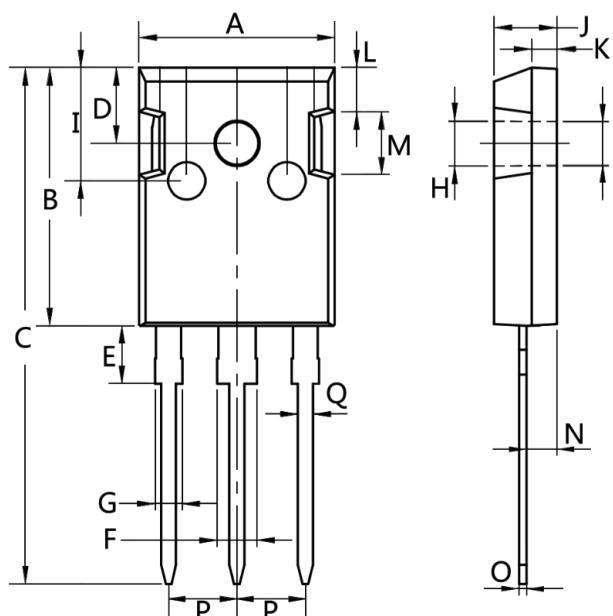


Figure 11. Normalized Maximum Transient Thermal Impedance

Package Dimensions

TO-247



Dim.	Min.	Max.
A	15.0	16.0
B	20.0	21.0
C	41.0	42.0
D	5.0	6.0
E	4.0	5.0
F	2.5	3.5
G	1.75	2.5
H	3.0	3.5
I	8.0	10.0
J	4.9	5.1
K	1.9	2.1
L	4.9	5.1
M	1.9	2.1
N	3.5	4.0
O	0.55	0.75
P	Typ 5.08	
Q	1.2	1.3

Revision History

Revision	Release	Remark
V1.0	2023/11/28	Initial Release

Disclaimer

The information given in this document describes the independent performance of the product, but similar performance is not guaranteed under other working conditions, and cannot be guaranteed when installed with other products or equipment. To achieve the required performance of the product in actual scenarios, the customer should conduct a complete application test to assess the functionality of the product.

Allpower assumes no responsibility for equipment failures result from using products at values that exceed the ratings, operating conditions, or other parameters listed in the product specifications.

The product described in this specification is not applicable for aerospace or other applications which requires high reliability. Customers using or selling these products for use in medical, life-saving, or life-sustaining applications do so at their own risk and agree to fully indemnify.

Due to product or technical improvements, the information described or contained herein may be changed without prior notice.